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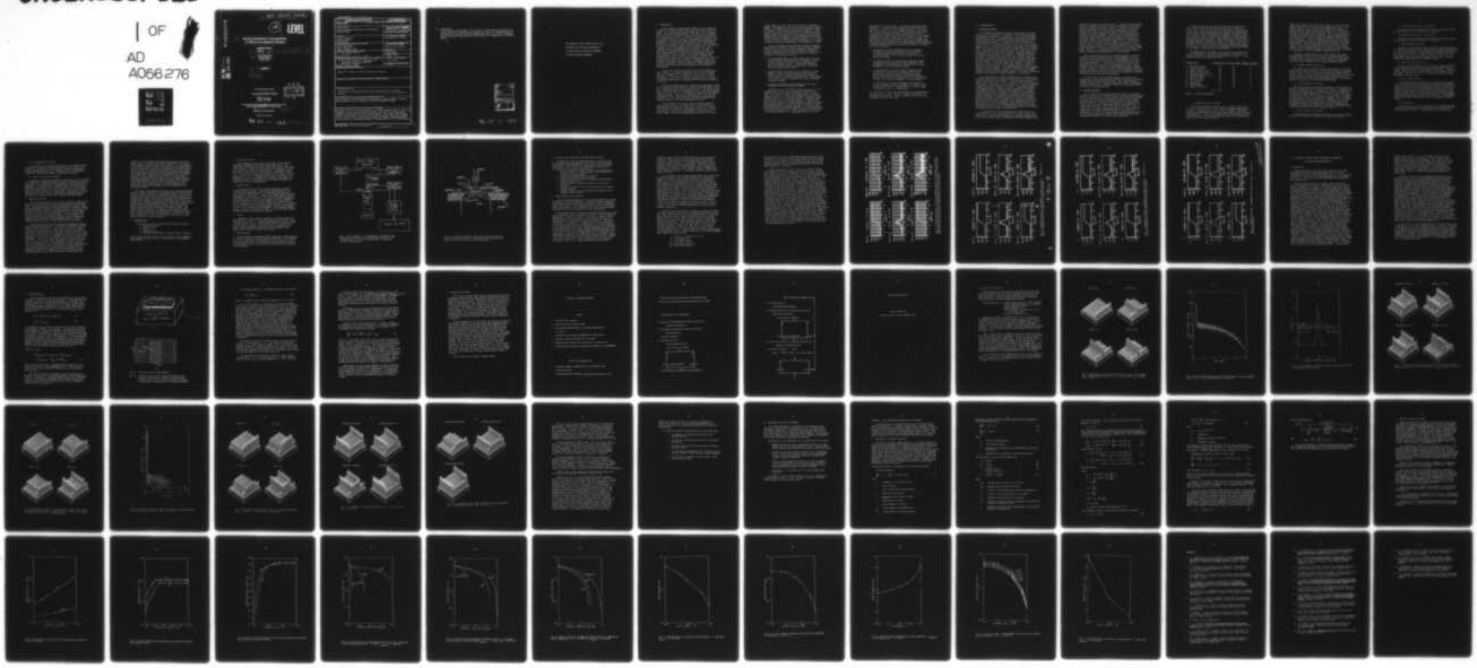

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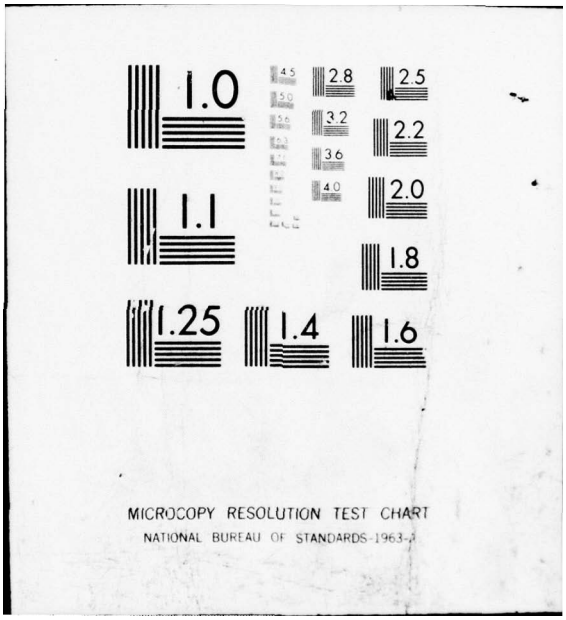
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The present report is the first portion of a second breakdown study of a specially designed array of silicon-on-sapphire diodes. The goal is to relate second breakdown susceptibility to device characteristics. The diodes, fabricated by Rockwell International, allow the roles of device doping, diode width, n-region length, junction spikes, metallization spikes, and current crowding geometries to be explored by a stroboscopic method. Exciting pulses of 0.1, 1 and 10 micro-

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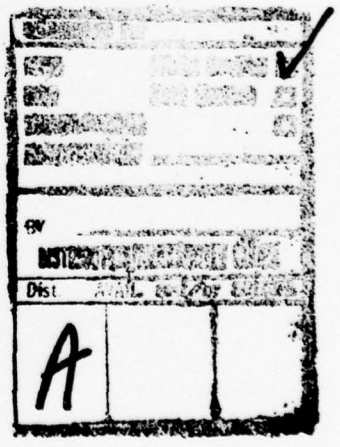
seconds duration are employed. At this date, the experiments have been set up, but the bulk of the experimentation remains to be done. A simplified model for describing the features of current filamentation that lead to second breakdown has been pursued in some depth, but this is also to be regarded as in an interim stage.



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I. INTRODUCTION

Second breakdown in semiconductor devices occurs through the formation of current filaments under sufficiently high electrical stress. The filamentation pattern depends upon device geometry, doping levels,and exciting waveform. The latter, in turn, depends upon the circuital constraints as well as the generator waveform. For a particular device in a particular circuital environment and a particular generator waveform, the filamentation pattern is very reproducible. This has been shown vividly in the experiments on SOS devices (1-5) and with bulk transistors (6-8). The filamentation pattern changes, however, when the exciting waveform changes. At present, many of the features of the initiation of current filaments and their subsequent growth are known. Yet, the combination of thermal and electrical effects is so complex in real, three-dimensional systems that device designers have only broad guidelines on how to design for minimum tendency toward filamentation. (These include: avoid current crowding, use relatively high doping in the high resistance region of the device, and allow for effective heat transfer.) Generally devices are designed with primary concern for their performance under normal circuital conditions; conditions leading to second breakdown are typically abnormal and are not encountered in the lifetime of most devices.

In those cases where susceptibility to second breakdown is a major concern, it is highly desirable to have a test arrangement that can distinguish the susceptibility of the device to second breakdown. If the test is to allow the selection of one device over another, then the test should be non-destructive. Attempts to develop non-destructive screening tests have not been successful in the past.

In second breakdown tests of a single device type under a fixed set of conditions, the transition to second breakdown tends to occur over a relatively narrow range for most devices. Occasionally, however, a "maverick" device will appear that has a much lower threshold. This has been attributed to the presence of geometrical and compositional deviations. These may be diffusion spikes associated with microscopic defects (dislocations and vacancies), a non-uniform distribution of the doping material, irregular definition of the diffusion windows, or to some combination of these.[9]

In three-dimensional devices, current filaments generally start in the interior of the device and it is very difficult to experimentally determine the course of the growth of a filament. For relatively low amplitude, long duration excitations, a rather broad hot spot is visible on the surface of the device prior to device damage. With increasing amplitude, melting occurs in the

central region of the hot spot and the device is permanently damaged. Two-dimensional thin film silicon-on-sapphire devices exhibit the formation of hot spots and subsequent melt formation similar to three-dimensional devices. However, in these devices the current path is parallel to the substrate and the heated regions can be observed in relationship to the junction geometry using a stroboscopic technique developed by Sunshine (10-13) and used by Budenstein, Smith and Pontius (1-5). This technique allows the dynamic growth of filaments to be observed in devices having major dimensions a few micrometers or larger.

Silicon-on-sapphire diodes have been specially designed and fabricated by Rockwell International's Electronic Research Division so that the roles of device geometry, deliberately created spikes and device base doping could be related to current filamentation for a range of excitation conditions.[14] The goals of the present effort are:

A. To perform experiments of a basic nature which will lead to an increased understanding of the nonlinear, electrothermal processes that cause current filamentation in silicon-on-sapphire diodes. Of particular concern are the roles of device geometry, doping levels, diffusion spikes and metallization spikes.

B. To develop analytical models for the influence of diode geometry, doping, diffusion spikes and metallization spikes on current filamentation under both forward and reverse biases in silicon-on-sapphire diodes. Such models will provide a basis for design of diodes more resistant to second breakdown.

C. To develop non-destructive screening tests for second breakdown in silicon-on-sapphire diodes.

Funding for the fulfillment of the above goals was to be divided into two parts, one extending from June, 1977 to December, 1977 and the other from January, 1978 to December, 1978. The ability to fulfill the tasks depended upon having equipment capable of producing the necessary high power, short duration pulses and of recording these in a convenient manner. This equipment was to be provided by the U. S. Army Missile Research and Development Command (MIRADCOM) at Redstone Arsenal. This equipment did not arrive until late in February of 1978. The Tektronix Digital Waveform Instrument, the central instrumentation package, had several defective circuit boards and was not operational until April 3, 1978. Because of the delay in receiving the equipment, the experimental objectives of the

program have yet to be pursued. The Tektronix Digital Waveform Instrument is a sophisticated, computer-controlled system that can process, as well as acquire, single-shot data. At the present time, we are still in the process of setting up the system for acquiring and processing data. Because of the delay in receiving the equipment, we requested an extension of the contract termination date from December 31, 1977 to March 31, 1978. This extension was granted. The present report is not intended as a final report on the proposed effort, but rather an interim report. A proposal has been submitted to the Army Research Office describing the work contemplated during the next twelve months. Its goals are stated as follows:

A. To assess the relative importances of device geometry, metallization and diffusion spikes, and device doping on second breakdown susceptibility for electrical excitation pulses of 0.1, 1 and 10 μs under both forward and reverse biases.

B. To apply the results of simultaneously observed filament configuration and voltage and current waveforms to the development of non-destructive screening test for second breakdown in silicon-on-sapphire diodes.

C. If time permits, to develop analytical models for the influences of diode geometry, doping, diffusion and metallization spikes on current filamentation under both forward and reverse biases in silicon-on-sapphire diodes. Such models should provide a basis for the design of diodes that are more resistant to second breakdown.

D. If time permits, to obtain temperature-time mappings of silicon-on-sapphire diodes as filaments are formed. Such mappings will serve as a further guide to the development of theoretical models of filamentation.

Section II of this report will describe the experimentation. The major effort to date, devoted to computer simulations, is presented in Section III. Section IV describes priorities and milestones for work during 1978.

II. EXPERIMENTATION

A. Stroboscopic Method

The stroboscopic method[1] is based on the decrease with temperature of optical transmittance through thin film silicon devices on transparent substrates. As temperature rises, high temperature regions appear darker. Experiments have been typically performed using constant current pulses with a pulse repetition rate of 10 to 100 pulses per second. A strobing arc lamp is flashed after a controlled time delay measured from the rise of each current pulse (Figs. 1 and 2). The device is located on the stage of an inverted microscope and its image is viewed with illumination by the strobing light. This light is an air arc source having a duration of 10 or 20 ns, depending upon the lamp being used. The image viewed with illumination by the strobe source reveals a temperature mapping of the diode during the period of illumination. Although the light is intense, 50,000 Watts at peak power, not sufficient energy is available to expose a photographic film with a single strobe flash. With specimens 1 μm thick and using the 20 ns lamp with ASA 3000 film, 50 flashes of the strobe light were required to obtain good exposures. Thus 50 separate current pulses had to be applied. When filamentation occurred, the filaments appeared as dark regions against a light background. Since each photograph is the integrated exposure of a large number of pulses, the fact that well-defined filaments appear on the photographs attests to the highly reproducible nature of the filaments for given conditions of excitation.

The interpretation of second breakdown effects is facilitated by using constant current pulses. The rationale for constant current testing was indicated by Sunshine.[10] Second breakdown produces a negative resistance region in the I-V characteristic at sufficiently high voltages. Thus there are two currents for a single voltage and a tendency to switch from one to the other. In constant current testing using pulses of fixed duration, the number and location of the filaments does not change as current amplitude is increased. (A different pattern of filaments occurs when the pulse length of constant current pulses is changed.) Although an intuitive view of the miltiplicity of filaments has been given with the constant current constraint, the matter remains to be treated rigorously. Double-step (single current pulse with two current levels) experiments provide an interesting result: the filamentation pattern of the first part of the step changes to that characteristic of the second part in a time of a few mircoseconds from the second step. The transition time is just the thermal time constant of the system connected with heat transfer to the substrate.

In constant current pulse testing, the voltage follows the current waveform at low levels when there is no appreciable temperature rise. As the current amplitude is increased, heating occurs in the junction and n regions, requiring an increased voltage at the

terminals to sustain the constant current. Filament formation lowers the device impedance and hence leads to a decrease in the terminal voltage to sustain the constant current. A two-step current pulse during filamentation thus can be used to approximate a constant voltage pulse. Also, in constant voltage testing, one does not anticipate a stable filamentation pattern. Two reservations must follow the previous statement: they are based on observations on relatively large devices (500 μm device width) and on pulses 5 μs and longer (longer than the thermal time constant of the device). The present study is concerned with pulses of 0.1, 1 and 10 μs and the first two are shorter than the thermal time constant of the system. Thus, if constant current pulses as short as 0.1 μs yield stable filamentation patterns, it is uncertain what constant voltage pulses will yield. The present experiments will try to explore this point. However, it is very difficult to obtain constant current pulses of hundreds of milliamperes and 0.1 μs duration.

One of the goals of the present experimentation is to provide a basis for screening tests that will allow measurement of the threshold of second breakdown without causing damage to the device. As pulses become shorter, they must be of higher amplitude to produce second breakdown. At the same time, the difference in pulse amplitude from that of the onset of filamentation to that of melt formation tends to decrease as the pulse width decreases. However, it may be possible to assess the second breakdown susceptibility of a system at relatively long pulse lengths if the continuity of behavior between short and long pulses can be properly established. This will be explored during the present experiments.

To perform the stroboscopic experiments on the time scale required and to obtain the desired information requires more advanced equipment than that previously employed. This includes optical system, improved pulser, improved stroboscopic source, and improved recording and processing equipment. These will be discussed further in Section IID, Instrumentation.

B. SOS Test Specimens

The test array of diodes have been fabricated in two separate batches at the Electronics Research Center of Rockwell International.[14] All of the sapphire wafers were cut from a single boule and polished on both sides. Wafers were purchased from Union Carbide with an epitaxial layer of silicon 0.6 μm thick and with a single doping level of $10^{14}/cm^3$. The wafers were divided into two batches, with five wafers to a batch. Each batch contained one wafer at the doping levels 10^{14}, 10^{15}, 10^{16}, 10^{17}, and $5 \times 10^{17}/cm^3$. All were n-type, with the higher dopings being obtained by phosphorous ion implantation of the base $10^{14}/cm^3$ material. During each ion implantation a 1 cm^2 of the starting wafers was prepared in addition to the wafer for making the diodes. This square will serve as a calibration reference in the stroboscopic experiments.

The die size for the test array of diodes is 169 mils by 205 mils. Each die contains 214 test diodes and about 70 dies are on each wafer. Thus the two lots will contain about 150,000 diodes in all. All of the processing after the original ion implantations for adjusting the base dopings was done together for each of the two lots. Thus, if there is a significant difference produced through the processing, this will show up upon comparison of corresponding devices in the separate batches. Within each batch will be 70 devices of single geometry. Comparison of these will provide a check on the uniformity of processing over the surface of a single wafer. Rockwell has a test array on each die for providing materials parameters for the devices. From this they have generated a data packet similar to that used in characterizing their MOS devices.

The geometries of the diodes in the test array are shown in Ref. 14, the design report of Rockwell International. The diode test array is divided into structure types as indicated in Table 1. Each structure type will be discussed briefly.

Structure Type	Devices per Die	Dice per Wafer	Wafers per Batch
1. Standard reference	25	70	5
2. Enclosed reference	20	70	5
3. Contact spikes to p++	20	70	5
4. Contact spikes to n++	20	70	5
5. Diffusion spikes p++ to n	20	70	5
6. Diffusion spikes n++ to n	20	70	5
7. Miltiple spikes	51	70	5
8. Half size spikes	20	70	5
9. Hour terminal	6	70	5
10. Doping level	1	70	5
11. Interdigitated	2	70	5
12. Radius of curvature	9	70	5
Total	214		

TABLE 1. SOS DIODE STRUCTURES

1. Standard reference structures

The standard reference structures cover a range of diode widths (w = 10, 30, 100, 300, 500 μm) and a range of spacings between the p+ - n and n - n+ junctions (x_e = 1.2, 2, 4, 8, 20 mils). The widest diodes are the same width as those previously studied by Smith, Pontius and Budenstein.[1-5] These are included to provide continuity with previous experiments. The smallest width was chosen to be comparable in width to that of existing IC diodes.

Lengths were chosen so that, for large values of x_e, the depletion region during reverse bias would have a length less than x_e. The smallest value of x_e was chosen to be comparable to values in existing diodes. Tests on the standard diodes will include observation of the filamentation pattern for pulses of 0.1, 1 and 10 μs, recording voltage and current waveforms. The I-V characteristics of diodes for small applied voltages (no current filamentation) will be recorded prior to pulse testing and afterwards in those cases where melts occur. In order to develop screening tests, waveforms will be examined carefully for indications of the onset of current filamentation. Previous work indicates small changes in the slope of the voltage wave as filamentation starts and further voltage changes as the filaments grow across the length x_e. The waveforms will be recorded on magnetic memory; these waveforms may be processed to reveal power vs time, and d(energy added)/dt vs time.

Parameters explored in the above tests include pulse width, pulse amplitude, type of pulse, number of filaments, locations of filaments, device width, n-region length, ratio of n-region length to device width, threshold for onset of filamentation, threshold for onset of melt formation, device doping, and bias polarity.

2. Enclosed reference structures

The second set of reference structures is similar to the first except that the metallizations, p+ and n+ regions extend to the edges of the diode on the first, while these regions are islanded in the second. Similar tests to those above will be performed on these diodes. The corners of the islands serve as concentration centers for the current and hence influence the filamentation pattern. There are 20 diodes in this array, the 20 mil widths being absent.

3. Contact spikes to p++ region

One of the concerns of the present program is the evaluation of geometric irregularities at the metal-p++ interface. To explore this, spikes 5 μm high have been incorporated on a saw-tooth background of 1 μm height on diodes having n-region lengths of 10, 30, 100, 300, and 500 μm and diode widths of 1.2, 2, 4, 8, and 20 mils. The spikes are positioned about 1/3 of the distance from the edge of the diode so that they will not be in a position of symmetry. The 5 μm length was chosen because it was believed to be representative of spikes in "maverick" three-dimensional devices. The first stage in the investigation will be to compare the filamentation geometries and waveforms with those of the reference structures. Depending on what is observed, further tests will be made as required.

4. Contact spikes to n++ region

Concerns and device geometry are the same as in section 3 above, except that the spikes are located on the metal-n++ interface.

5. Diffusion spikes on p++ - n interface.

Concerns and device geometry are the same as in section 3 above, but the spikes are located on the p++ - n interface.

6. Diffusion spikes on n++ - n interface

Concerns and device geometry are the same as in section 3 above, but the spikes are located on the n++ - n interface.

7. Miltiple spike structures

Devices of a single width, 8 mils, and with n-region spacings of 10, 30 and 100 μm each contain 3 spikes of equal length on a background of 1 μm triangular spikes. Spike lengths for different diodes are 1, 2, 4 and 8 μm. Spikes are located in different diodes on one of the four interfaces: metal - p++, metal - n++, p++ - n, n++ - n. The group also contains reference structures with no spikes. Concerns are similar to those described in section 3 above.

8. Half-size spike structures

Devices of a single width, 4 mils, and with n-region spacings of 10, 30, 100, 300 and 500 μm each contain a single spike of 2.5 μm length located about 1/3 in from the edge of the device. Spikes are located in different diodes on one of the four interfaces: metal - p++, metal - n++, p++ - n, n++ - n. Concerns are similar to those described in section 3 above.

9. Four terminal devices

Diodes having n-region lengths of 10, 30 and 100 μm and widths of 1.2 and 4 mils have an extra set of electrodes on the n-region. A bias on these electrodes will influence the current pattern in the system and hence the current filamentation pattern. The structure allows one to control the degree of current crowding prior to the onset of filamentation. An exploratory period is necessary before a decision can be made on the most fruitful use of these structures. Obvious parameters include the ratio of cross-pulse to longitudinal pulse, pulse widths, diode widths, length of n-region, and device doping.

10. Doping level

A test structure is present in each die for measuring the sheet resistance of the n-material. This will be done in going from one die to another as a means of checking uniformity of processing.

11. Interdigitated structures

Two structures are available that simulate the geometry between fingers of a three-dimensional interdigitated device. These will provide some perspective on the pattern of current filamentation of the three-dimensional structure. Parameters that can be explored include n++ - p++ spacing, doping, and excitation waveform.

12. Radius of curvature structures

A sequence of diodes was designed to stimulate the current patterns in 3-dimensional diffused epitaxial transistors. Radius of curvature of the p++ and n++ islands and spacing between these islands were the parameters. The design sought to minimize series resistances while preserving the proximity of two regions of small radius of curvature. Radii of curvature for the p++ and n++ regions are 5, 10 and 30 μm, both radii being the same for a single diode. Separations of the two regions are 10, 30 and 100 μm. Parameters to be explored include pulse duration, radius of curvature, n-region width and doping.

C. Temperature mapping

The stroboscopic method can be used for temperature mapping of an SOS device at any time during or after application of the exciting pulse. Qualitative data are readily obtained by photographic means. However, quantitative data are much more difficult to obtain. Hence, strong motivation is needed for considering such an undertaking. The motivation is associated with the design question: how to design devices so that they are most resistant to second breakdown (while still meeting other design specifications). If time permits, we propose to make dynamic temperature mappings during filamentation, thereby providing designers with experimental data in a simple geometry which can be used as reference in model calculations.

The possibility of performing quantitative temperature mapping has already been demonstrated.[4] The standard arrangement for photographic recording is modified. In the film plane of the camera is placed on opaque screen with a small hole in its center. Behind this hole is a photomultiplier. The light passing through the hole comes from a small portion of the specimen. A ten-mil aperture and magnification of 100 implies a specimen viewing area that is 0.1 mils in diameter. The size of the aperture in practice, is taken as a compromise. If it is too large, then details of filamentation are lost. If it is too small. then the transmitted light is so little that the temperature range for measurements is severely limited. To obtain a temperature profile, the device is moved across the optic axis of the microscope, while supplying current pulses and appropriately positioned strobing pulses, and the amplitudes of the transmitted pulses are recorded as a function of device position. The method would be quite simple except for a complication; the

intensity of the strobing light differs appreciably from flash to flash. Thus the transmitted intensity depends both on the specimen absorption and the incident light intensity. An investigation of the incident light intensity for different strobe pulses showed that the intensity distribution was approximately a Poisson distribution and that the fluctuations from pulse to pulse were random. The method adopted previously for making quantitative measurements was to apply about 1000 pulses at a fixed position of the device, record each pulse transmitted with the aid of a pulse height analyzer, and obtain from the output of the pulse height analyzer the average amplitude of the transmitted pulses. About one week of work was required to scan across a single diode at a single delay time of the strobing light. Thus, the possibility of quantitative mapping was demonstrated, but the method was prohibitively tedious.

The present instrumentation system and the stroboscopic method provide a unique capability for temperature mapping if an alternate scheme is used for observing the transmitted pulses. Light of the incident strobe source may be divided with a beam splitter prior to reaching the specimen, with one portion serving as a reference beam and the other transmitted through the specimen. The ratio of the transmitted to reference beam measures the temperature. The Tektronix digital waveform instrument may be used to record the reference signal and the transmitted signal, convert each to digital form, select the maximum of each and compute the desired ratio. The operation may be repeated for a number of pulses and an average taken. With an appropriate stepping system to translate the specimen, a single scan could be accomplished in a few minutes. The device could then be returned to its initial position, the strobe delay adjusted and another scan made.

D. Instrumentation

A stroboscopic experiment includes the following subsystems:

1. Stroboscopic source
2. Optical system
3. Pulser
4. Synchronization
5. Recording oscillographic system and signal processor

These will be described briefly in this section. A block diagram of the arrangement is shown in Fig. 1, with a detail of the specimen region of Fig. 2.

1. Stroboscopic source

The stroboscopic source must be an intense, short duration, dependably triggerable, repetitive, white light source. The source that will be used is a Xenon Corporation air arc lamp having a peak output of 50,000 watts and width at half maximum of 10 ns. The regular power supply for this lamp uses a triggerable voltage that rises from 0 to 10 kV in 100 μs and the lamp fires at about 6 kV. Jitter arises because the lamp may fire one time at 5 kV and another at 6 or 7 kV. A Pulspak 10 power supply modified by its manufacturer for the low impedance arc lamp has a rise time of 10 ns from 0 to 10 kV, so that the jitter on firing is probably not measureable with our instrumentation.

2. Optical system

To obtain the best optical resolution requires a properly integrated optical system. A Reichert MeF metallograph is to be used in the new experiments with a transmitted light objective corrected for a cover slide. The ten-mil sapphire substrate closely approximates the thickness of a glass cover slide commonly used in transmission optical microscopy. The system includes a transmitted light condensing lens system, since maximum resolution depends on the phase coherence of the incident light on the system and this, in turn, depends on both the source characteristics and the condenser. With a 40X objective and the condensing lens system, a resolution of about .4 μm is theoretically obtainable. The filaments observed using 5 μs pulses previously were about 5 μm wide and those created by shorter pulses will probably be narrower.

3. Pulser

High power, high frequency transistors are now available that make possible a constant current pulser that operates at 700 V with risetimes of about 5 ns. In addition MIRADCOM has supplied, on loan, a Velonics Model 380 pulser that provides constant voltage pulses. The two pulsers (constant current and constant voltage) will be used to compare filamentation patterns in the unexplored time regime short compared to thermal time constant.

4. Synchronization

The stroboscopic arrangement requires appropriate synchronization of the device pulse with the stroboscopic light pulse. This requires inclusion of appropriate delay pulses to take into account delay in the strobe power supply. The time that the strobe fires is observed by a photodiode and a marker pulse is put onto either the voltage or current waveform.

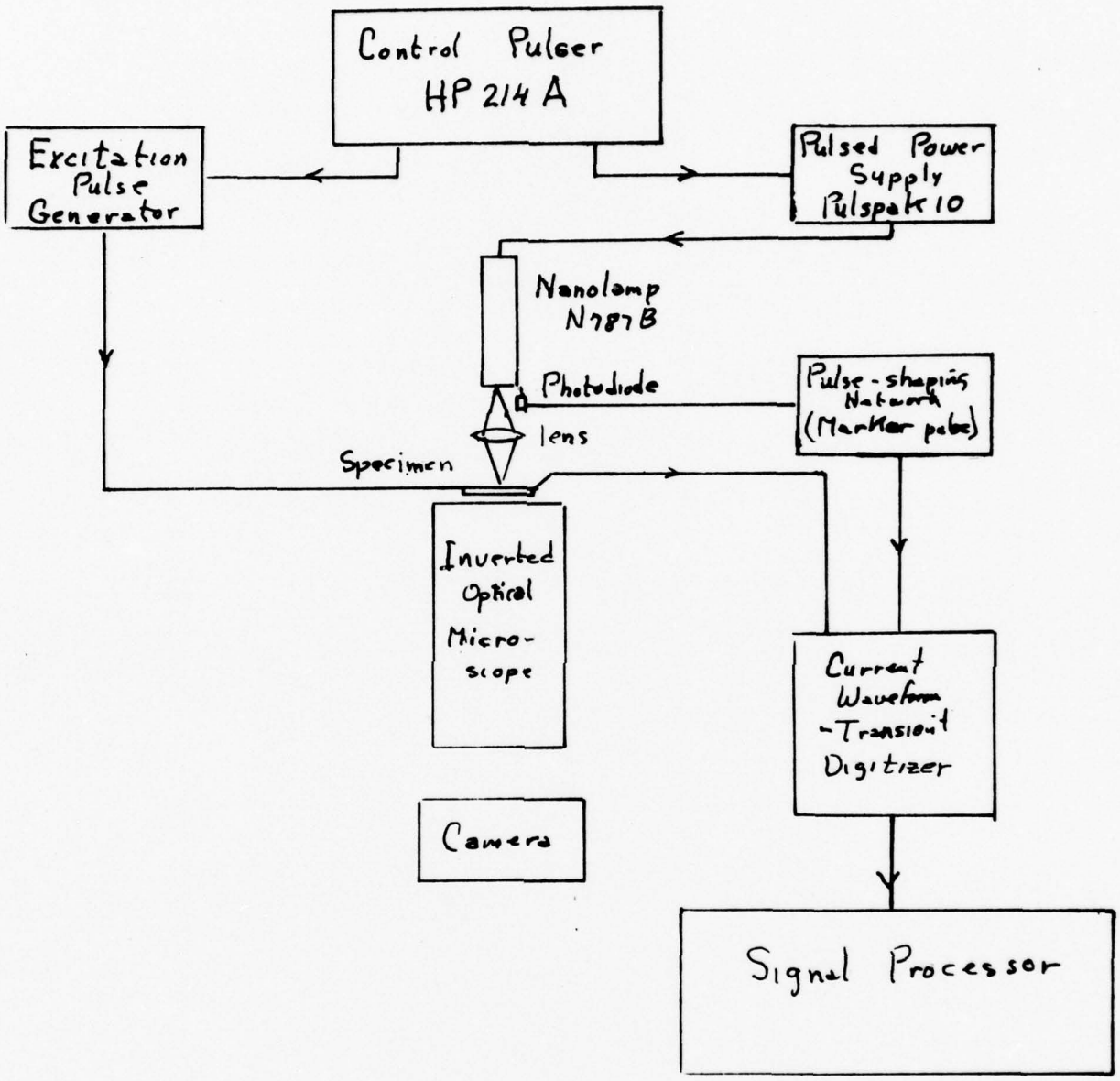


Fig. 1. Block diagram of the stroboscopic arrangement using photographic recording of the filamentation pattern and the Tektronix digital waveform instrument (DWI) for waveform recording and processing.

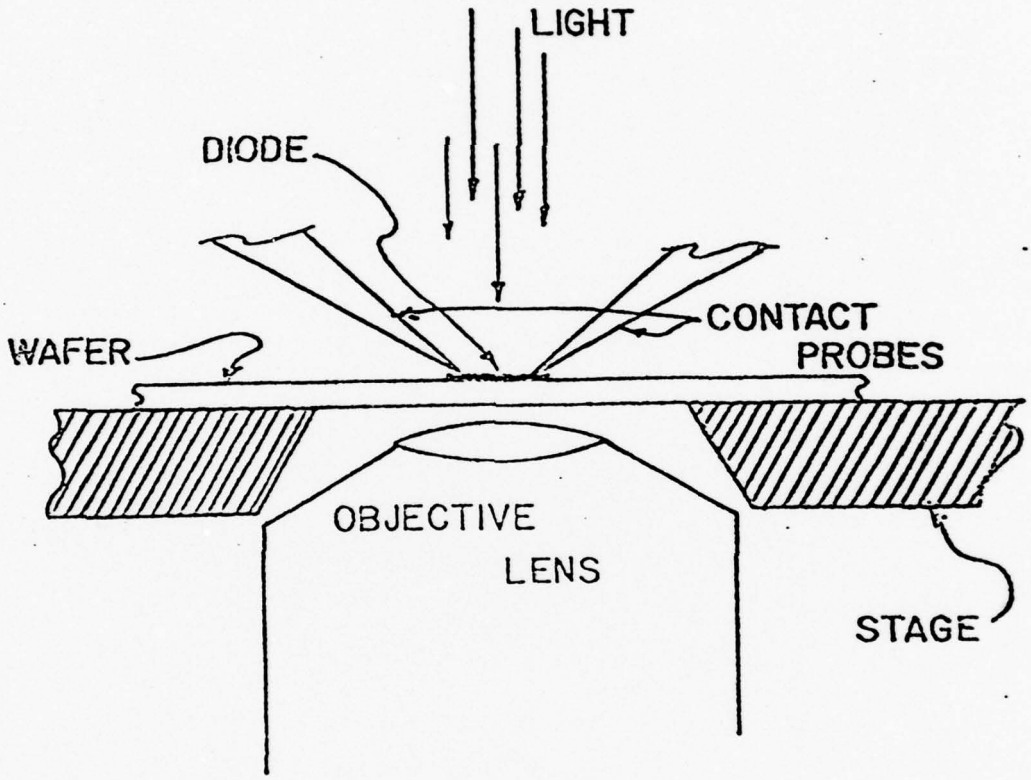


Fig. 2. A silicon-on-sapphire diode in position for observation of second breakdown phenomena. The wafer, probes and stage are moved as a unit to select the area of observation.

5. Recording oscillographic system and signal processor.

The Tektronix Digital Waveform Instrument is ideally suited for recording and processing single-shot events on the time scale of interest in these experiments. The system can accept multiple input signals, requiring one 7912 input waveform digitizer for each signal. The system, more specifically,

1. records the incident pulse in digital form (sampling the pulse 512 times in a single pulse for pulses as short as 5 ns and as long as 1000 μs)
2. displays the incident pulse on a monitor
3. stores the digital record of the pulse
4. processes the incident pulse as directed (differentation, Fourier analysis, etc.)
5. processes pulses from several sources in its central processor
6. displays the output of the central processor on a graphics display terminal
7. provides a hard copy of the information displayed on the graphics display terminal.

E. Data Acquisition and Analysis

First, a brief explanation of how the system works will be given. with the R7912 transient digitizer. The R7912 transient digitizer contains the controls which govern the display of the incoming waveform. These controls include vertical and horizontal scale factors, method of triggering, trace intensity, focus, and z-axis modulation. The waveform itself is displayed on the 632 video monitor.

The transient digitizer contains a specially-designed tube called a scan converter which is composed of a matrix of silicon diodes on a single chip. The chip is 1.3 cm x 0.95 cm with a density of about 800 diodes per linear centimenter. On one side of the chip is a reading gun and on the opposite side is a writing gun. The diodes are either in an uncharged or a charged condition corresponding to the written or unwritten state, respectively. The charge condition of the diodes may be changed by the writing beam, which is modulated by the incoming waveform. Thus, waveform information may be stored on the diode array in the form of charged and uncharged diodes, that is, in digital form. This information may then be obtained by the reading gun to be sent to the 4165 controller or for display on the video monitor, depending on controls sent from the keyboard. Because of the finite width of the trace there will usually be two vertical points for each horizontal point, corresponding to the upper and lower edges of the trace. Once the waveform is digitized into

controller memory it may be stored permanently on one of the two floppy disks and it may be operated upon by the TEK SPS BASIC functions. "TEK SPS BASIC" is a modified BASIC language which includes special functions to, for example, communicate with the transient digitizer, display graphics data, and process string functions. The waveform, other waveforms, tables, comments, and so forth may be displayed on the graphics terminal in almost any manner desired by the user. This graphic display may then be hard-copied, if needed.

It was desired to have a BASIC program which would acquire the necessary waveforms, perform the appropriate data corrections, assign a file name to the waveform, and store the waveform on a floppy disk. The program which was written for this purpose is not listed here but a description of it is given below. The program contains two subroutines; the first acquires correction data to be used by the second and the second is a general purpose waveform acquisition routine. In more detail, the first subroutine searches the scan converter tube for defective diodes and identifies these diodes in an array. Then a dot graticule is displayed on the video monitor and digitized into controller memory. The digitized dot graticule is compared to the instrument's internally generated electronic dot graticule and tables of horizontal and vertical constants are prepared to correct for electron beam distortion Finally, the subroutine acquires a zero-reference trace, that is, a trace with the input grounded, and returns control to the main program. (The input is grounded manually with a switch on the transient digitizer.)

The main program is designed to acquire two waveforms, assign them file names, and store them on the floppy disk under the given file names. The first part of the program obtains the current waveform. Statements on the display screen indicate that a current waveform is to be stored. When the user is ready to input the waveform he presses a key which transfers control to the waveform acquisition subroutine. This subroutine rejects defects, finds the best average of the upper and lower edges of the trace, and performs the geometry correction. Then control is returned to the main program and a series of questions are printed on the terminal asking the user to input a letter and several numbers which are concatenated to give a waveform file name of the format AQBCCDDEE. These symbols are defined below.

Q - Current or voltage ("C" or "V")
A - Lot number (1,2)
B - Wafer number (1-5)
CC - Die number (01-70)
DD - Structure type (01-14)
EE - Diode number (01-51)

Any comment about the particular waveform may be typed in at the terminal and it will be stored with the waveform and in a special file reserved for comments. The program stores the waveform and comments and proceeds to repeat the steps outlined above for the voltage waveform. After the waveform is stored the program ends and is ready to be run again.

Another program was written to take two waveforms, compute their derivatives, their product, and the derivative of the product, making a total of six waveforms. If the original waveforms are current and voltage vs. time then the other four waveforms will be the derivatives of current and voltage vs. time, power vs. time, and the derivative of power vs. time. It was found that the original waveforms and their product presented no problem but the three derivatives were filled with random noise, as seen in Fig. 3. Taking an average of the original waveforms ten times seemed to be a logical way to reduce the noise. The results of this approach are shown in the second diagram. The noise is reduced but it still considerably distorts the derivative waveforms. The third diagram shows the result of averaging the waveforms one hundred times (this takes about twenty minutes to run). There is only a slight improvement over the average of ten waveforms. At this point it was recognized that the problem was not simply noise. The vertical and horizontal scales are not continuous; as the waveform increases (decreases) there is a point where it must move to the next higher (lower) scan line. Since there are only 512 horizontal points and 512 possible vertical points, considerable distortion is introduced when the derivative is computed. To minimize this distortion, two separate arrays were set up to compute the derivatives. These arrays contained only 51 points each, every tenth point of the original arrays. The purpose was to make the array small enough so that the vertical distance between adjacent points would be large compared to the distance between scan lines. The results of using a 51 point array to compute the derivatives is shown in the fourth diagram. Experiments with arrays of different sizes showed that the 51 point array offered the best compromise between reducing distortion and eliminating information.

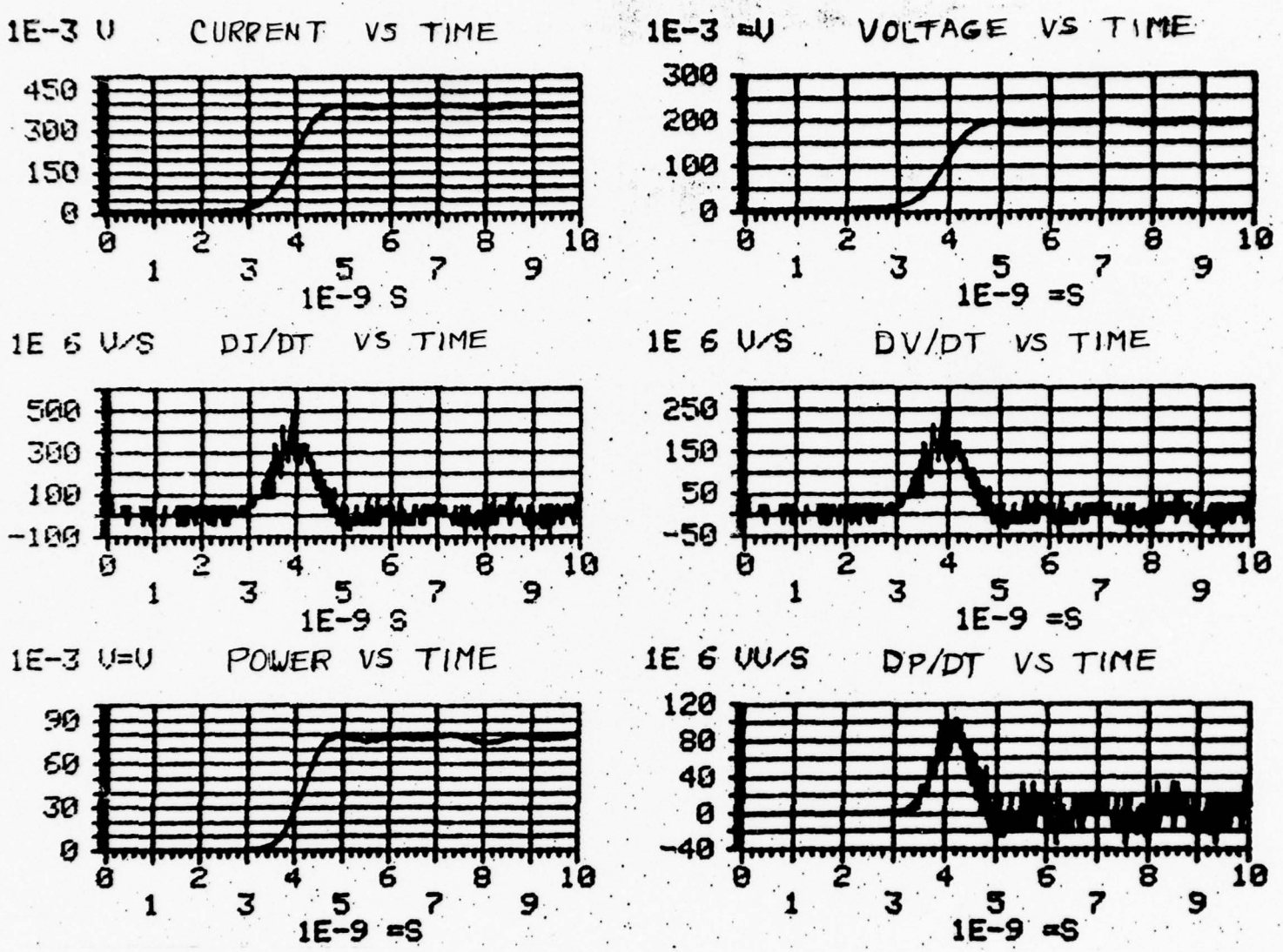


Fig. 3. Waveform processing. The two waveforms taken from the Tektronix transient digitizer are at the top, their derivatives in the second row, their product on the lower left and the derivative of their product on the lower right.

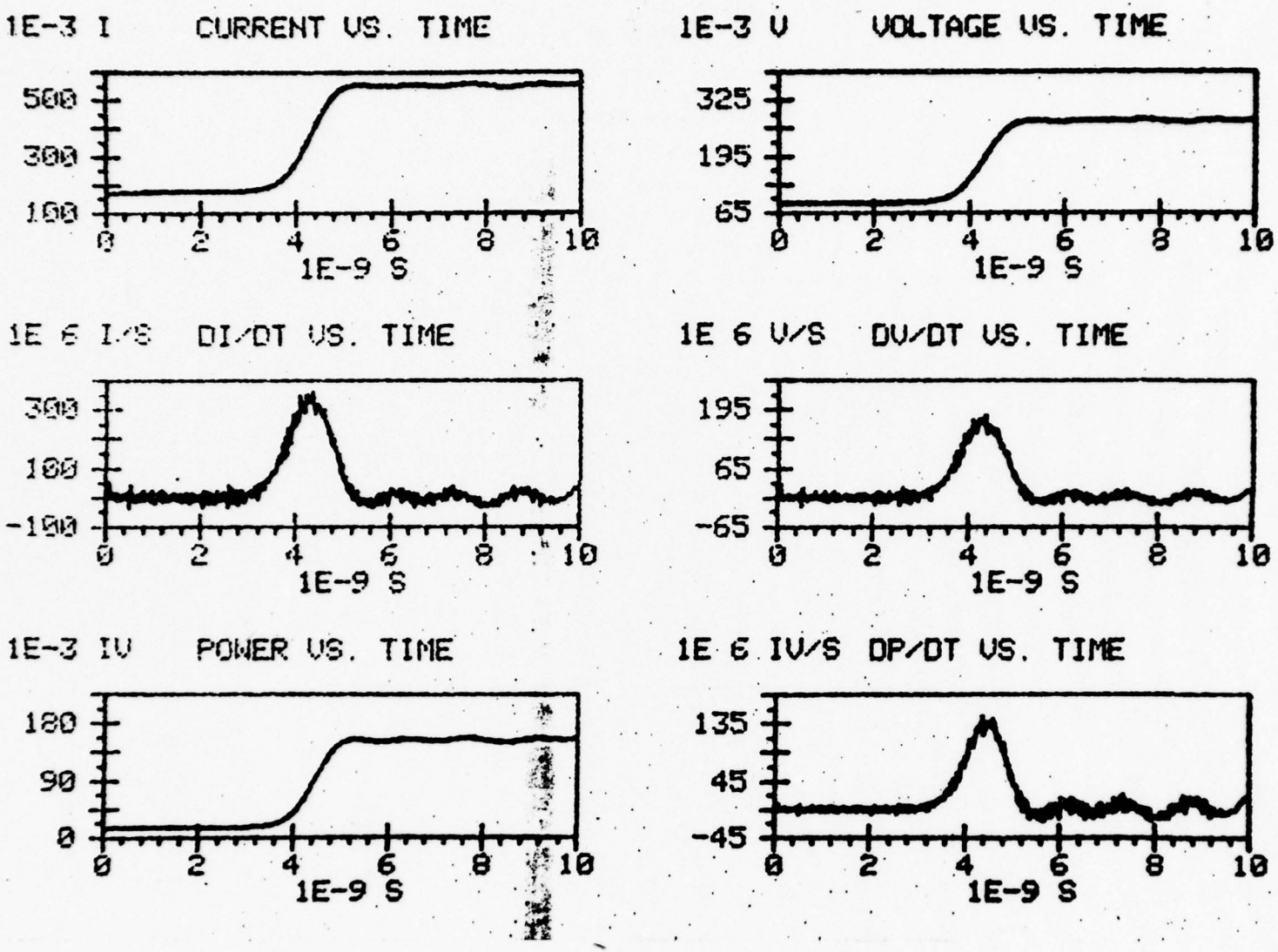


Fig. 4. Waveform processing. Arrangement the same as in Fig. 3. However, the original waveforms are the averages of 10 separate waveforms.

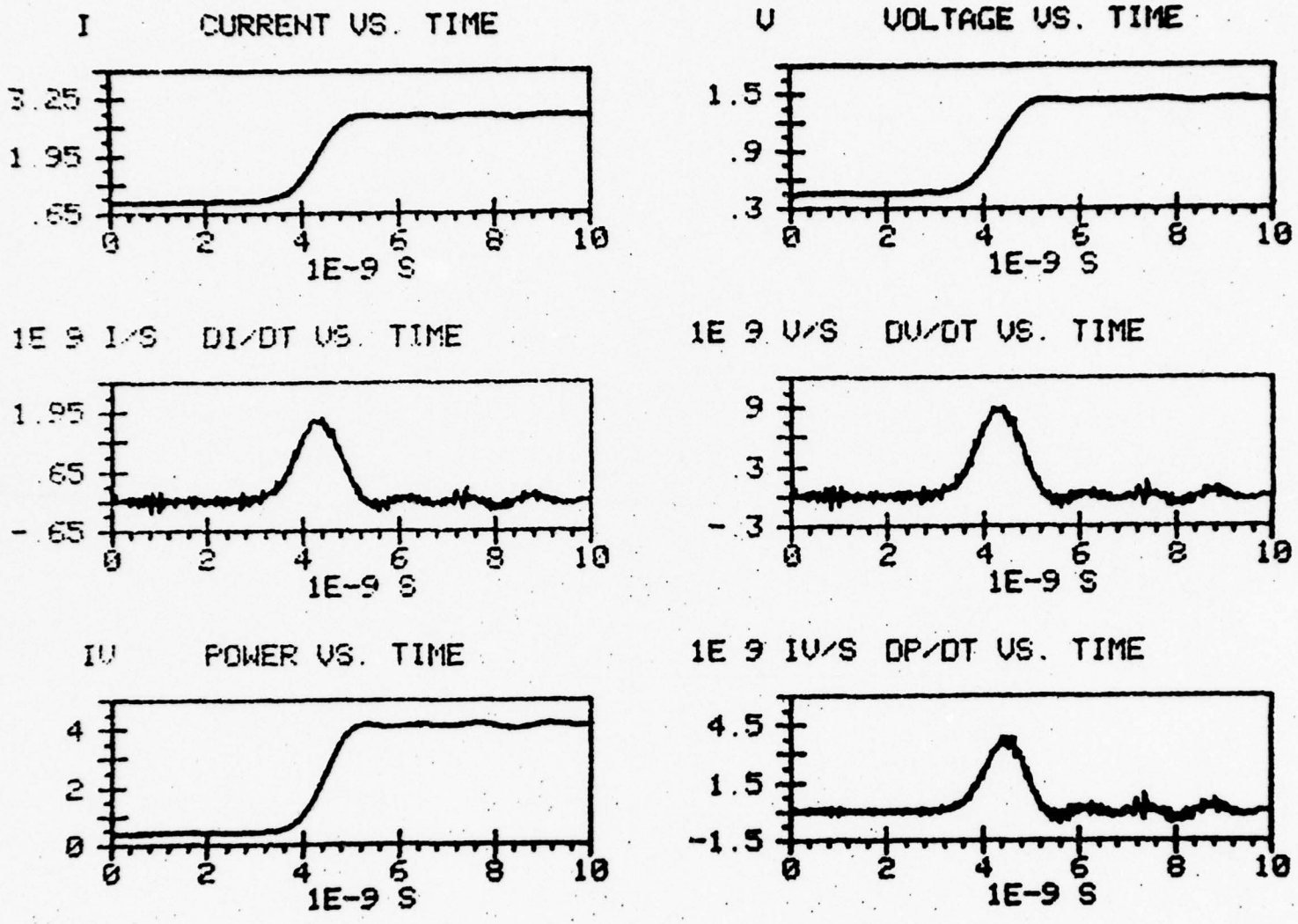


Fig. 5. Waveform processing. Arrangement the same as in Fig. 3. However, the original waveforms are the averages of 100 separate waveforms.

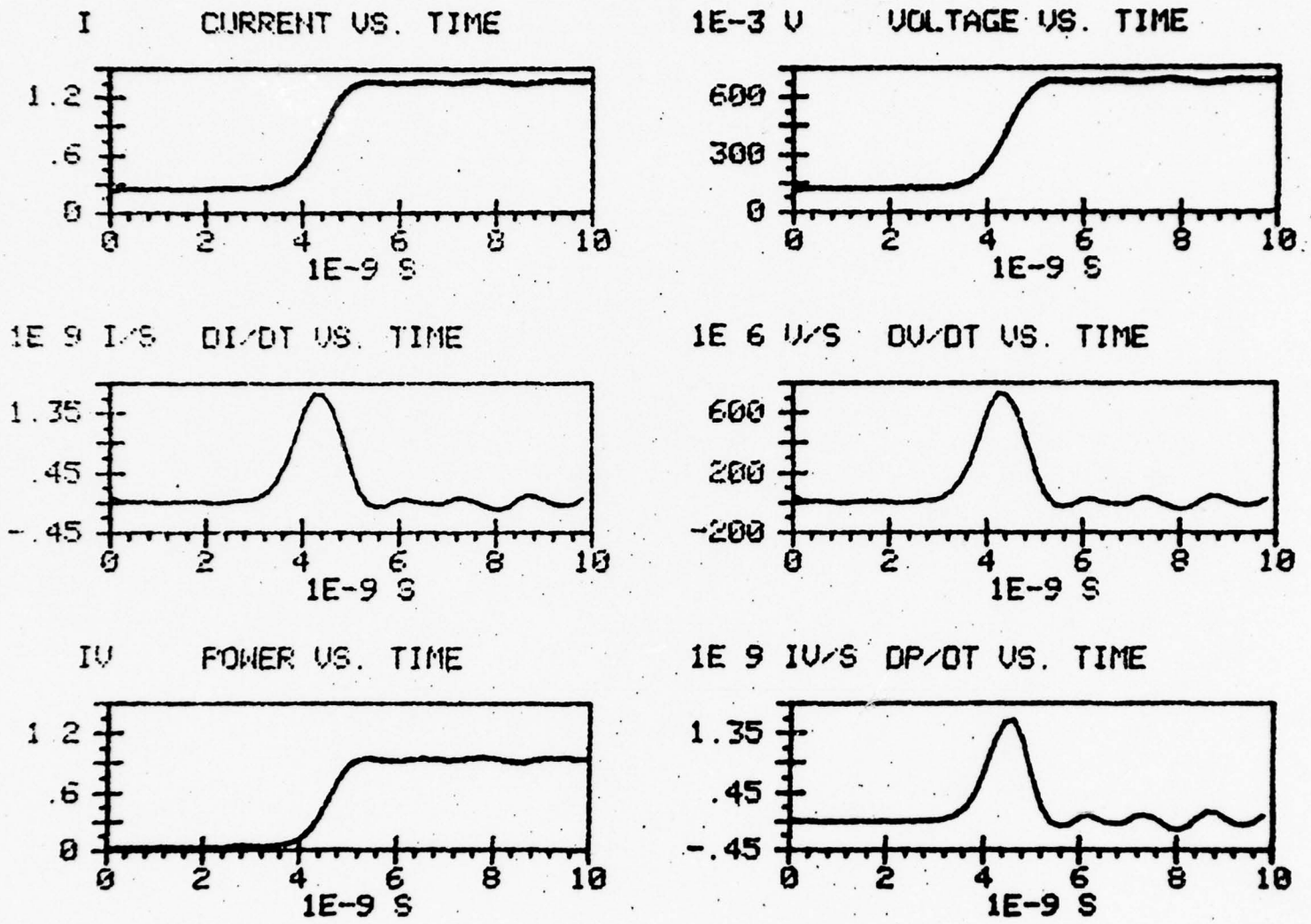


Fig. 6. Waveform processing. Arrangement the same as in Fig. 3. See text for smoothing procedure.

III. A SIMPLFIED COMPUTER MODEL FOR CURRENT FILAMENTATION IN SILICON-ON-SAPPHIRE DEVICES

A. Background

Second breakdown in SOS diodes under reverse bias has been explained as an electrothermal phenomenon involving current filamentation (6,7,10). For diodes having a p+ - n - n+ structure, the regions of most concern in second breakdown are, for reverse bias, the p+ - n junction and the n region and, for forward bias, the n region alone.

When a strong current step is applied under reverse bias, there is appreciable increase in temperature first in the junction region and then in the n region. The initial temperature rise in the junction region is accompanied by a ballasting effect because avalanche becomes more difficult at higher temperatures, indicated by the higher voltage needed for maintaining the same device current. Also, the n region itself has a stabilizing effect associated with the positive temperature coefficient of resistivity above room temperature for several hundred degrees (depending upon doping level). This also tends to increase the terminal voltage necessary for sustaining a constant current. Eventually the temperature in some portion of the junction becomes high enough that the number of thermally generated carriers introduced into the junction becomes significant. The junction voltage then drops and more current passes through the hot region, which, in turn, becomes still hotter. The junction voltage locally drops nearly to zero and the current increases still further since the device voltage does not change greatly. The vanishing of the junction voltage causes current from the surronding region to funnel through at the hot spot. The size of this region is limited by the spreading resistance associated with the lengthened current paths of the converging current filaments. Eventually another portion of the junction will become hot enough for start of a filament. Thus multiple filaments form. The n region heats up within the locales having concentrations of current and, at sufficiently high temperatures, experiences a negative temperature coefficient of resistivity due to thermally generated carriers. This becomes increasingly unstable and a broad, hot current filament grows across the n region for each junction filament. As a filament grows across the n region, there is still a portion of the current streamlines that goes through cool material where the temperature coefficient of resistivity is positive. This portion provides a ballasting effect for the filament. However, when a filament ultimately bridges the n region, then it no longer has a ballast and the current increases rapidly. A narrow melt

channel forms along the axis of the filament and grows rapidly outward as the current is sustained. This melt produces the damage associated with second breakdown. For a constant current step, the device voltage increases during the early stages, drops slightly as filaments are initiated but then continues to rise as the n region is heated in the temperature interval where resistivity increases with temperature. As the filaments grow across the n region the voltage drops and, upon formation of the melt filament, there is a sudden and considerable additional voltage drop.

A complete theory of second breakdown should describe all of the above in terms of the material properties and device geometry, giving potential, current and temperature maps and the device voltage as functions of time (assuming a constant current excitation step). Simultaneous solution of Poisson's equation, the continuity equation, and heat conduction equation is required using the appropriate constitutive equations and boundary conditions. Even with silicon-on-sapphire devices, the current distribution is two-dimensional in the plane of the film, while the heat conduction problem is three-dimensional. Elaborate computer solutions have been developed elsewhere (15-20), but these are very demanding of computer time. The demand becomes even more severe in the second breakdown problem than in other situations because the smallness of the current filaments forces one to use a fine spatial mesh and very small time increments. Thus, there seems to be little hope of exploring second breakdown effects via computer simulation unless appreciable simplification of the theoretical equations is made. In the past, simplifications have been made by focusing attention on a restricted aspect of the overall problem (for example, the onset of a hot spot at the junction (10), the transition from a hot broad filament to a melt channel (16), filament growth in a homogeneous system (2), the adiabatic problem (21), and a one dimensional current analysis (22)). Each of the special solutions provides some special, useful insight. None, however, have sufficiently wide scope to give the desired broad perspective.

In this section, another simplified model for describing current filamentation in a silicon-on-sapphire diode is presented. The intent of the model is to provide improved perspective on the role of junction irregularities on current under reverse bias in planar diodes. The model can be applied for different circuital constraints and it yields device waveforms, temperature distributions, and other detailed information. The model is an outgrowth of one developed by Pontius (1) to describe current filamentation in a thin homogeneous silicon film on a sapphire substrate.

B. Simplified Model

A thin film diode of the type to be analyzed is shown in Figs. 7a and 7b. The model divides the diode into J strips extending from one metallization to the other metallization. In addition, the n region of each strip is subdivided into K regions. A step current of amplitude I_{total} is applied at t=0. The voltage across each of the J strips must be the same value, $\Delta V(t)$, at any instant (Eq. 1), while the sum of the current of J strips equals I_{total} at each instant (Eq. 2).

$$\Delta V_j = \Delta V(t) \text{ for all values of } j \tag{1}$$

$$\sum_j I_j(t) = I_{total} \tag{2}$$

A one-dimensional description is used for the electrical conduction in each strip. However, the properties of the junction and of the other segments are temperature dependent. The solution is carried out in a two-step progression, first the electrical problem and then the thermal. At time t=0, the temperature of all parts of the diode is constant and equal to that of the substrate. The current divides equally among all the strips. The thermal portion of the problem is solved by equating the increase in internal energy in each small segment to the sum of the Joule heating during the previous time interval τ and the algebraic sum of the heat added to that element from the four surrounding elements and substrate (Eq. 3).

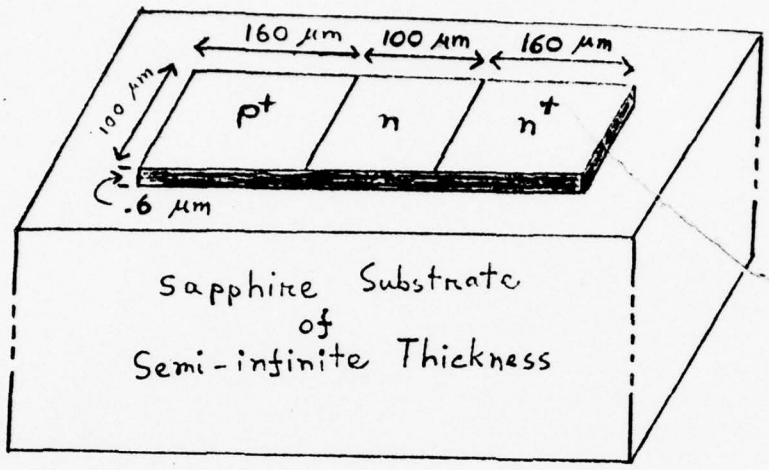
$$(c_m \Delta T)_{j,k} = \Delta Q_{j,k}$$

$$= \Delta Q_{j,k+1,j,k} + \Delta Q_{j,k-1,j,k} + \Delta Q_{j+1,k,j,k}$$

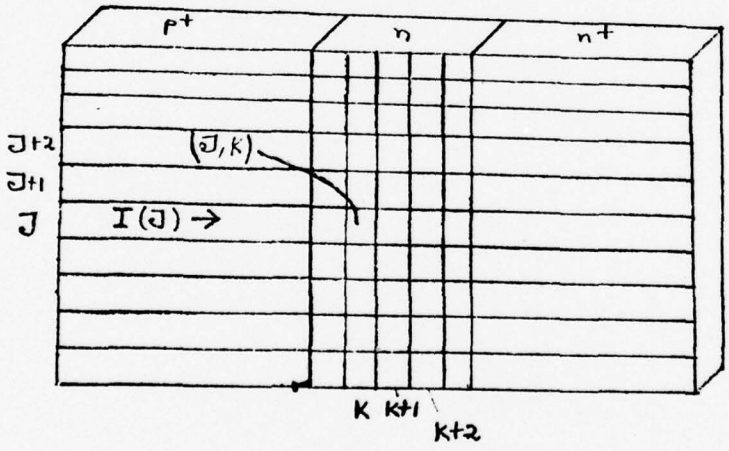
$$+ \Delta Q_{j-1,k,j,k} - \Delta Q_{Ts,j,k} + I_j^2 R_{j,k} \tau \tag{3}$$

The first four terms in Eq. 3 represent the heat gained by any strip from its four nearest neighboring strips. The fifth term is the heat lost into the substrate, while the last term expresses Joule heating.

The edge of the device is assumed to stay at constant temperature. This leads to a temperature gradient between longitudinal strips. An additional temperature gradient arises along each strip because of the thermal dissipation at the junction (reverse bias condition) and the higher resistivity of the n region compared to that of the p+ and n+ regions.



a



b

Fig. 7a. Silicon-on-sapphire diode geometry.

Fig. 7b. Division of silicon thin film into elements for the purpose of calculations. Each of the longitudinal strips (J index) is 4 μm in width, while the n-region is transversal, subdivided into 5 μm regions (K index).

The voltage across the J th longitudinal strip can be written

$$\Delta V_j = \sum_k \Delta V_{j,k} \quad , \tag{4}$$

where K is summed over the individual elements of the J th strip.

All of the K elements are temperature sensitive resistances except for the element on the n side adjacent to the p+ - n junction. This element contains the depletion region and, under reverse bias and low temperature, accounts for much of the voltage drop across the entire strip. The voltage across the junction is obtained with the usual one-dimensional theory of the abrupt p - n junction (23). However, the second breakdown problem involves the junction at unusually high current densities and unusually high temperatures. The high current densities lead to distinctive charge and field distributions, such that, at very high current densities, the junction voltage decreases even for isothermal solutions. As temperature rises, thermally generated carriers entering the junction become increasingly significant and the junction voltage drops toward zero at all current densities with sufficiently large rise in temperature. The junction characterisitics had to be calculated because they are not presented elsewhere over the broad ranges of temperature, current density, and n region doping needed for the second breakdown problem. These calculations are described in Appendix A.

The SOS diode considered was 100 μm wide, 420 μm long and has a silicon film thickness of .7 μm. The sapphire substrate was assumed to be of semi-infinite thickness. The n region was 100 μm long and contained 25 longitudinal strips each 4 μm in width. Each longitudinal strip was further divided into 22 segments 5 μm long. Thus any small segment is identified by two subscripts J and K, where J is the row number and K the column (Fig. 7b).

The SOS diodes were subjected to constant current pulses of amplitude from 15 to 35 mA and duration 5-15 μs. These currents lead to current densities during filamentation of 10^8 - 10^{10} A/m^2.

For lateral heat flow terms $\Delta Q_{j+1,k,j,k}$ and $\Delta Q_{j-1,k,j,k}$ the heat transfer parameter k_e is defined as k_{si}/(Segment dimension). See Eq.5 below. To calculate heat transfer into the substrate, parameter k_e is set equal to k_{sa}/(an effective film thickness). For ease in calculations, the various effective distances were adjusted such that the value of k_e for all of the above terms is the same while still maintaining their individual k's and their effective distances.

Programming was done in fortran language using an IMB 370/158 machine. A complete two-dimensional solution for a given current step requires an average of 7 minutes of computer time and 124K of memory for pulses. To keep the model simple and minimize computer time, multiple iterations were avoided whenever possible. Time step and grid size were maintained relatively coarse to obtain faster turnaround at the cost of better accuracy.

The heat transfer coefficients of Eq. 3 strongly influence the temperature and current distributions. To avoid the complexity of solving the heat conduction equation, heat transfer in Eq. 3 is described by a simple law of cooling

$$\frac{dQ}{dt} = -kA\left(\frac{T - T_{sur}}{x}\right) = k_e A(T - T_{sur}) \qquad (5)$$

where k is the thermal conductivity, A is the area through which the heat transfer takes place, x an effective distance between the element (which is at temperature T) and the source or sink close by (which is at the temperature T_{sur}). The thermal conductivity for silicon is about 108 watt/(m-K) and that of sapphire 22 W/m-K at moderate temperatures. The temperature dependence of the thermal conductivities has not been included in the present calculations but this can be added with comparative ease. The k values obtained from these and "reasonable" estimates of A and x yielded solutions that were not consistent with filamentation experiments. Thus k_e was taken as a heat transfer parameter and its values adjusted to make the calculated results be similar to experimental ones. Further work has to be done on this aspect of the solution.

Computations for a particular simulation run were terminated if device terminal voltage dropped suddenly and remained at a low level (signifying completion of filamentation), if computation become meaningless due to lack of convergence, or if temperature in any portion of the device reached that of the melting point of silicon, 1683 K (at which time permanent damage to the device occurs).

C. Computation Procedure

A set of initial conditions is selected: doping density of the n region, current amplitude, heat transfer coefficients, number of longitudinal strips, initial temperature, length of the time increments and the pulse duration. The current at first divides evenly among the longitudinal strips, because all strips are assumed to have the same properties. The voltage across the diode is, by Eq. 4, the sum of the incremental voltages across each portion of a single strip. Once the strip currents and incremental voltages are determined, Eq. 3 is used to determine the temperature rise in each element. The new temperature of each element is the old temperature plus the temperature change. Using this temperature and the known resistance-temperature relation, the new resistance is computed.

The new temperatures are not uniform over the diode because of the boundary condition at the diode edge (edge temperature equals that of the substrate) and the high temperature produced by the avalanching (reverse bias assumed) diode in the junction region. Thus the current distribution will no longer be uniform and an iterative procedure is required to determine how the current is distributed after the first time increment has passed. This cannot be accomplished analytically because the junction voltage depends not only on the junction temperature but also on the junction current density. Thus, a trial current distribution is first assumed. This distribution is constructed so that the total current in all strips is that specified by the current step amplitude. Each strip voltage is then computed. If these differ by more than some predetermined amount, then a new current distribution is tried. The process is repeated until all strip voltages are equal. Generally, the number of trial solutions is less than five. The new temperatures are then computed and the process repeated.

The structure of the computer program follows.

Structure of Computer Program

Time=0

1. Initialize all constants
2. Specify the size of spatial mesh
3. Set all mesh elements equal to substrate temperature,

   T_s = 293 K
4. Calculate total resistance STPRS(J) for every strip J
5. Calculate junction voltage VJ(J) for every J
6. Equally divide current ITOT along every J to obtain I(J)
7. Determine device terminal voltage from VTOT=VJ(J) + I(J)*STPRS(J)

Start Time Increment Loop

1. Calculate change in temperature due to electrical and

   thermal processes

   DT(J,K)=(DQ(J,K))/(stripmass x specific heat capacity of Si)

Where DQ(J,K)=heat gained from surrounding strips

-heat lost to the substrate+joule heating due to current

Calculation of new temperature

1. Calculate new temperature for every strip T(J,K)

   T(J,K)=T(J,K)+DT(J,K)

2. Calculate new resistance R(J,K) at new T(J,K)

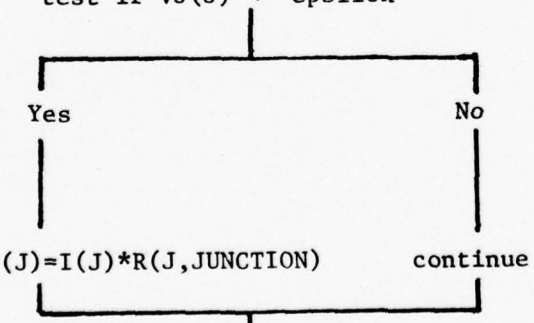
   R(J,K)=f(T(J,K))

   and hence STPRS(J)

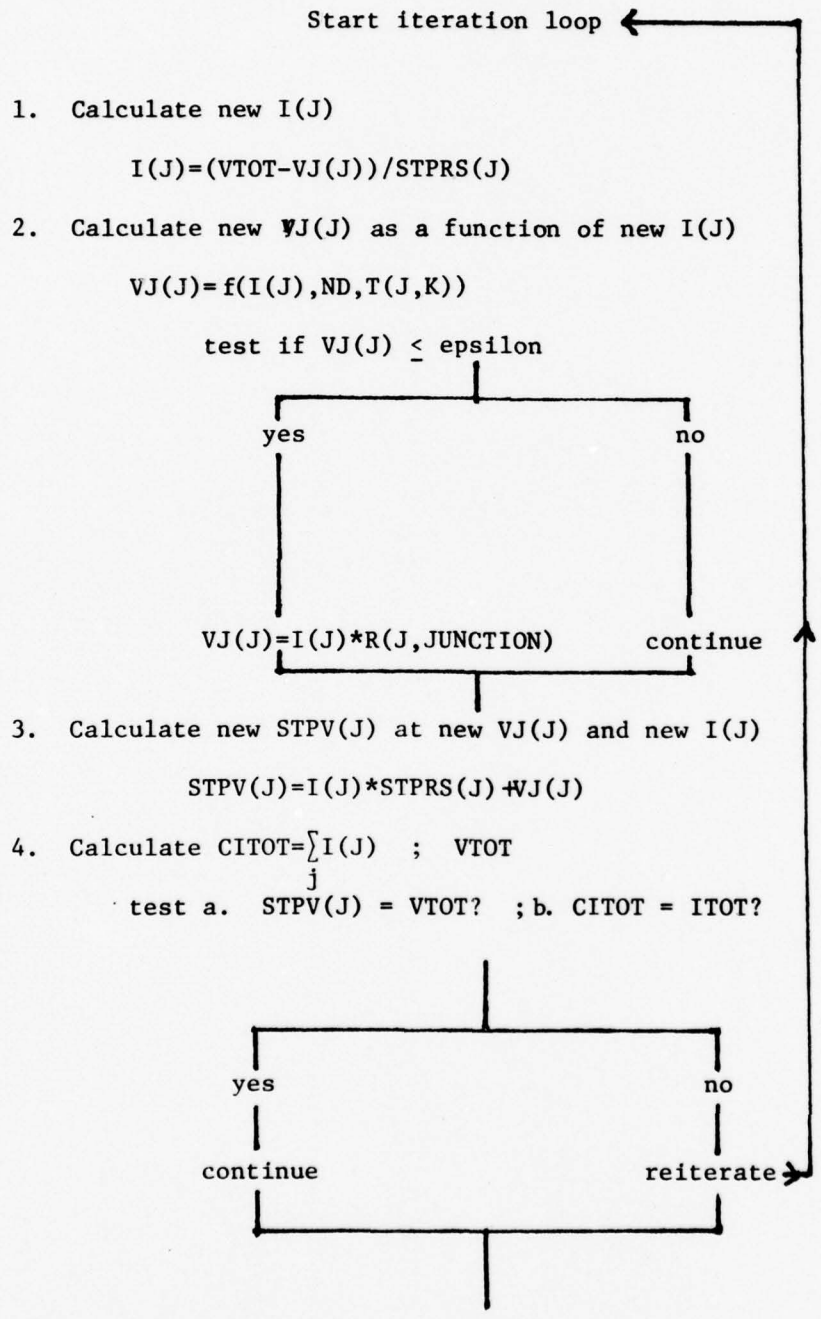
3. Calculate new VJ(J)

   VJ(J)=f(I(J),ND,T(J,K))

   test if VJ(J) <= epsilon



5. $VTOT=ITOT+\sum_{j}(VJ)J)/STPRS(J)))/\sum_{j}(1/STPRS(J))$


Start iteration loop
1. Calculate new I(J)
I(J)=(VTOT-VJ(J))/STPRS(J)
2. Calculate new VJ(J) as a function of new I(J)
VJ(J)=f(I(J),ND,T(J,K))
test if VJ(J) ≤ epsilon
yes
no
VJ(J)=I(J)*R(J,JUNCTION)
continue
3. Calculate new STPV(J) at new VJ(J) and new I(J)
STPV(J)=I(J)*STPRS(J)+VJ(J)
4. Calculate CITOT=∑I(J) ; VTOT
j
test a. STPV(J) = VTOT? ; b. CITOT = ITOT?
yes
no
continue
reiterate

Finish iteration loop

Time = Time + Tau

Go back to start of time increment loop

D. Results and Discussion

Some representative results will be presented here. The electrical conductivity of the n+ and p+ regions is sufficiently high that these regions experience little temperature rise during the times of interest. Thus the figures will show only the junction and n-region while describing temperature profiles.

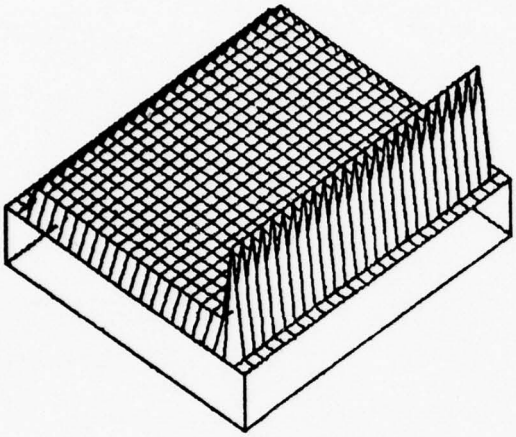
Diode parameters are: n-region doping density 1×10^{22} atoms/m^3
Current amplitudes 15mA, 25 mA and 35 mA
Initial temperature 293 K
Time increments 10^{-7} s
Thermal transfer parameter 0.05, 0.06, 0.07, 0.08, 0.10
Diode film thickness .6 μm

Temperature profiles at times of 0.79, 13.2, 14.4 and 14.7 μs are shown in Fig. 8 for a pulse amplitude of 15 mA. The junction region heats up rapidly, with the n-region lagging behind. At 0.79 μs, the n-region away from the junction is uniform in temperature except for the fall off at the edges of the device and at the n - n+ interface. A broad filament gradually forms and becomes progressively narrower. This transition is shown in the thermal profiles at 13.2, 14,4 and 14.7 μs.

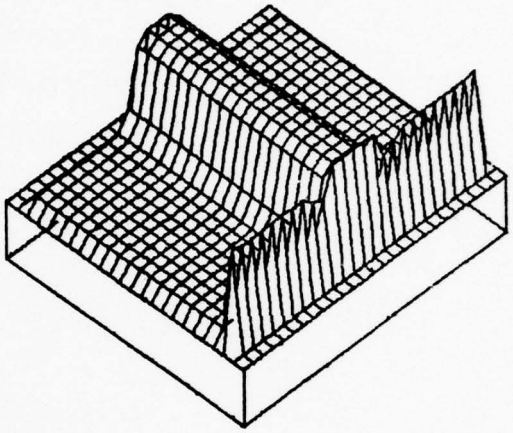
Fig. 9 shows the device terminal voltage as a function of time. The initial voltage step corresponds to the onset of the current step with the diode at ambient temperature. As soon as heating starts, there is an increase of voltage because of the initial rise in resistivity with temperature in the n-region and the decrease with temperature of the avalanche coefficients. The voltage peak at about 1.1 μs occurs as the temperature in the n-region becomes that of the peak of the temperature-resistivity curve. Beyond this temperature, resistivity decreases with increasing temperature. The oscillations are an idiosyncracy of the program which will have to be removed.

Fig. 10 shows the current distribution in each of the strips at times t = 0+, 1.1 μs (corresponding to the peak of voltage waveform), 3.1 μs (corresponding to the time when the voltage levels off after the peak), 5 μs, 10 μs and 15 μs.

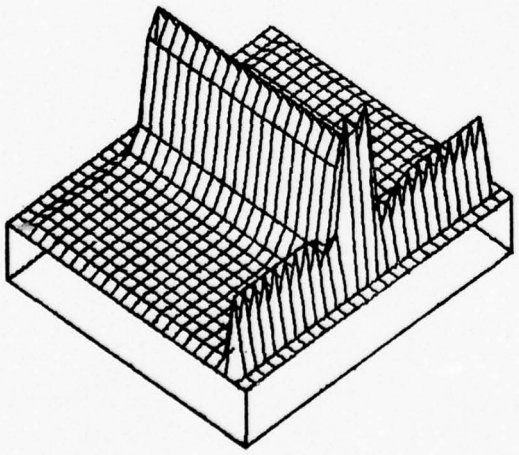
time=.79 μs



time=13.2 μs



time=14.4 μs



time=14.7 μs

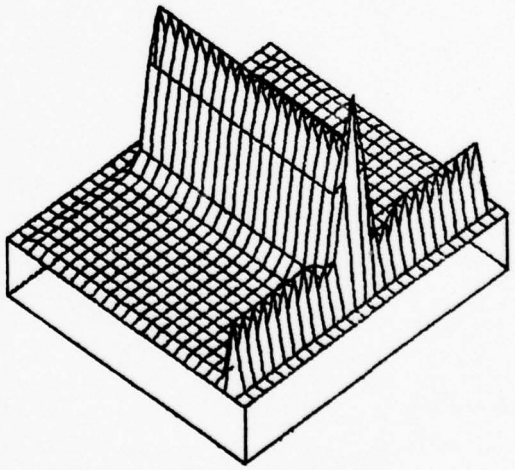


Fig. 8 Temperature profiles of an SOS device at various times leading upto a single filament formation. k_e = .10 watt/(m-K), I_{tot} = 15 mA, ND= 1 x 10^{22} m^{-3} .

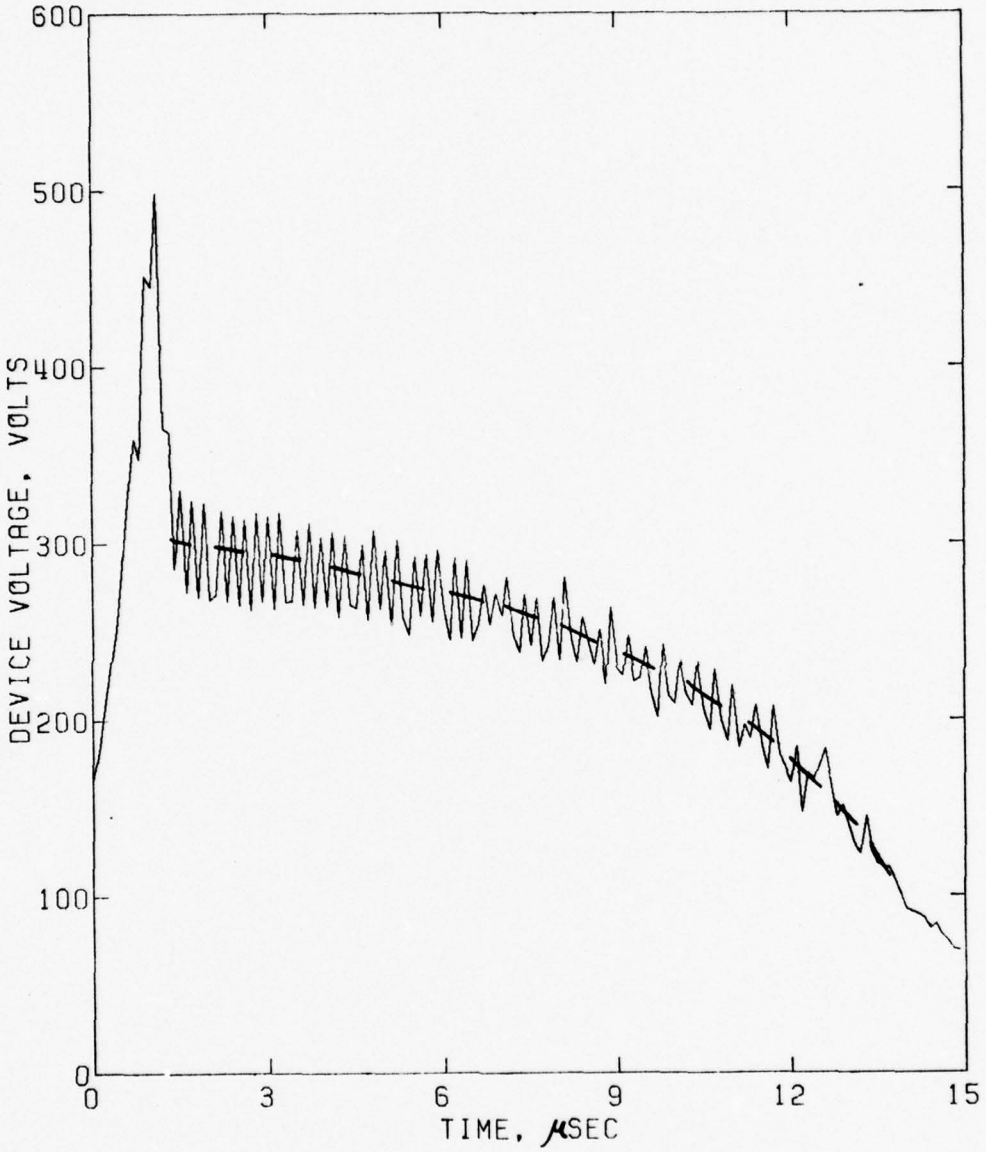


Fig. 9 Device terminal voltage as a function of time for a pulse amplitude of 15 mA. k_e = .10 watt/(m-K) and ND = 1 x 10^{22} m^{-3}.

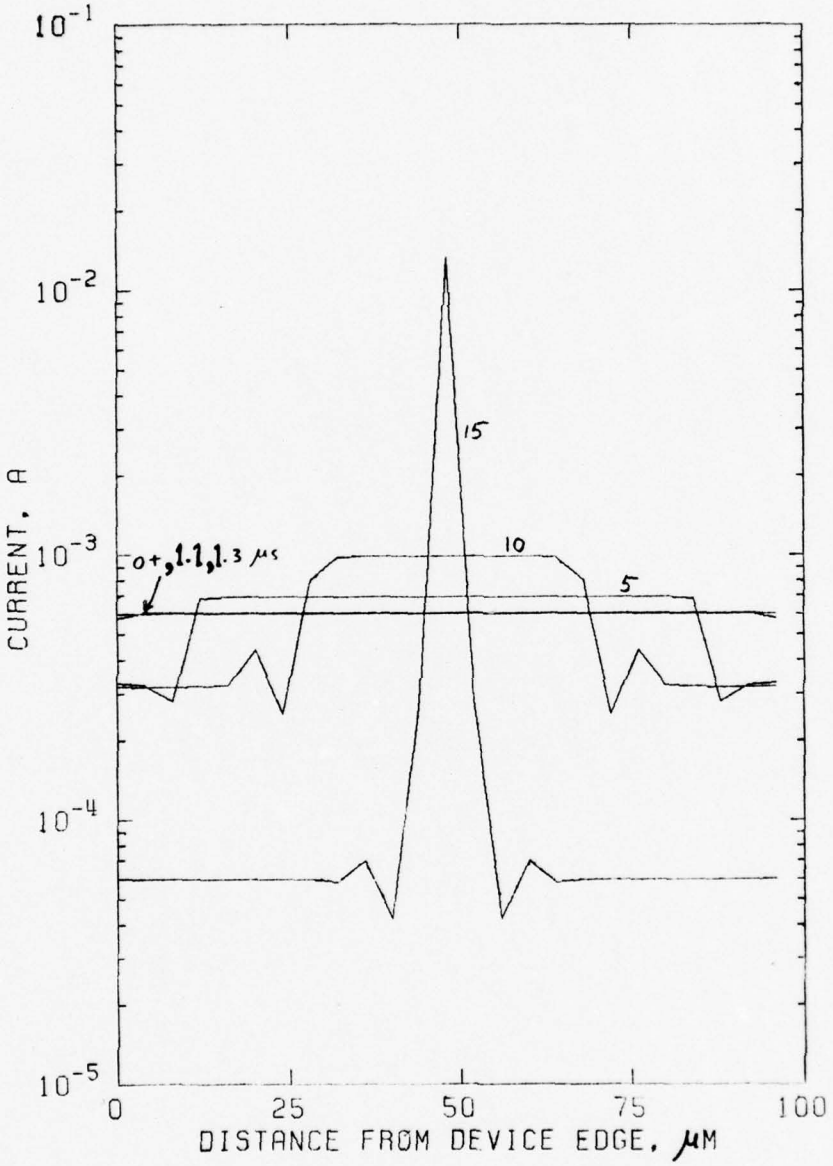
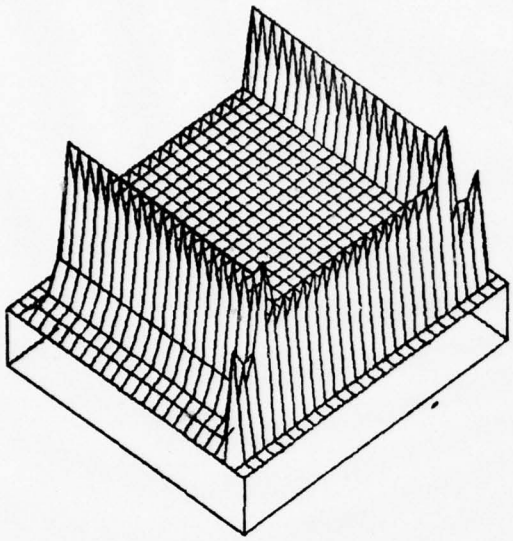
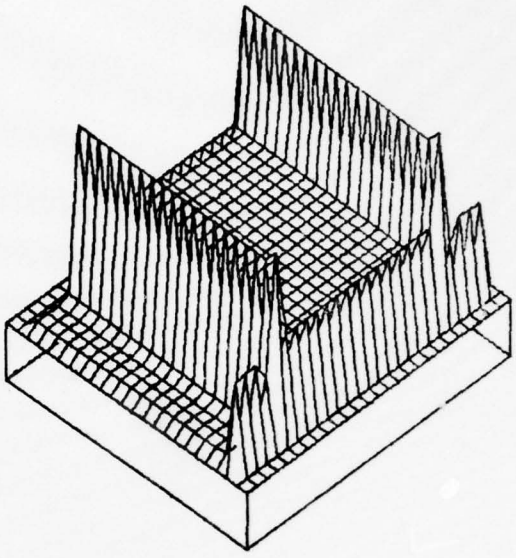


Fig. 10. Current profiles during a constant current step of 15 mA for the diode of Figs. 8 and 9.

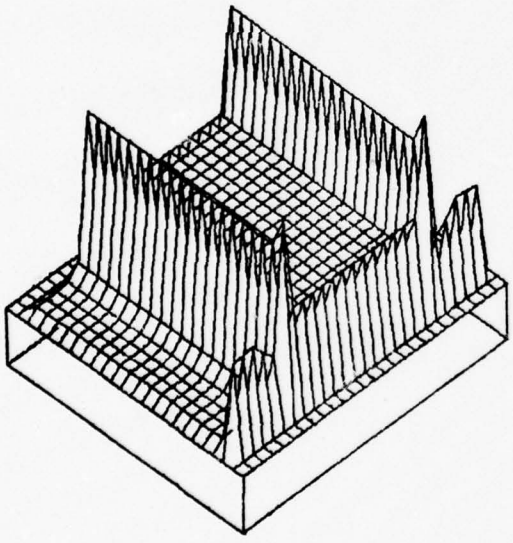
I=25 MA, K_e=.05 W/M K



I=25 MA, K_e=.07 W/M K



I=25 MA, K_e=.08 W/M K



I=25 MA, K_e=.10 W/M K

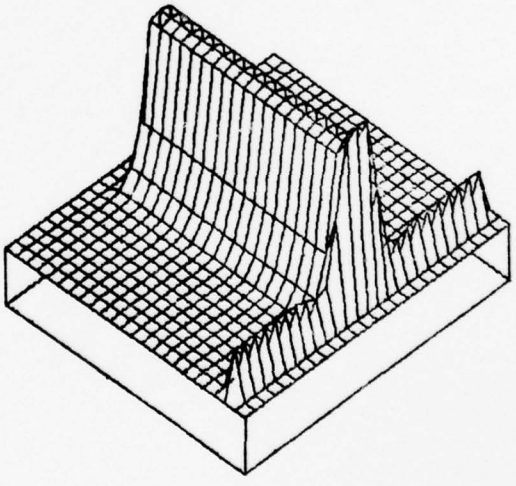
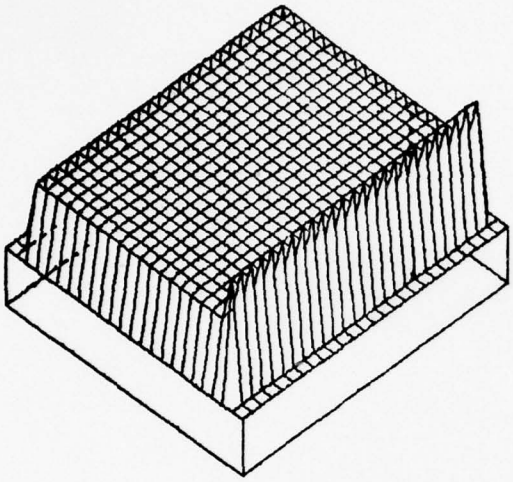
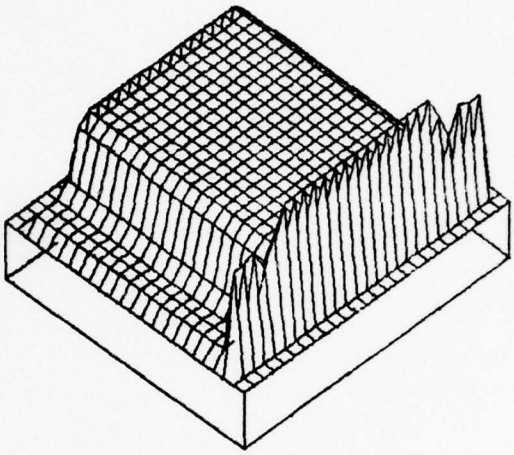


Fig. 11. Temperature profiles of an SOS device at various k_e values showing both single and double filamentation I_{total} = 25 mA, ND_e = 1 x 10^{22} m^{-3}

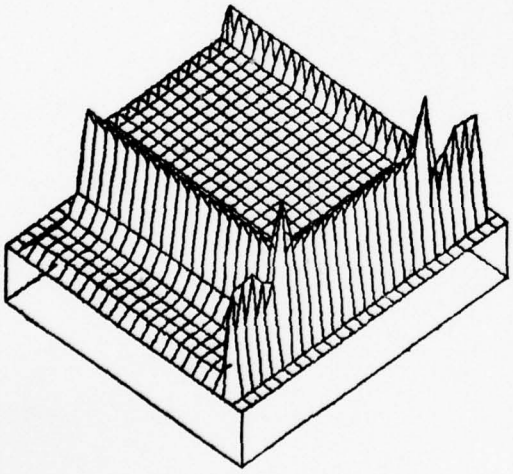
time=.8 μs



time=6.8 μs



time=7.9 μs



time=8.5 μs

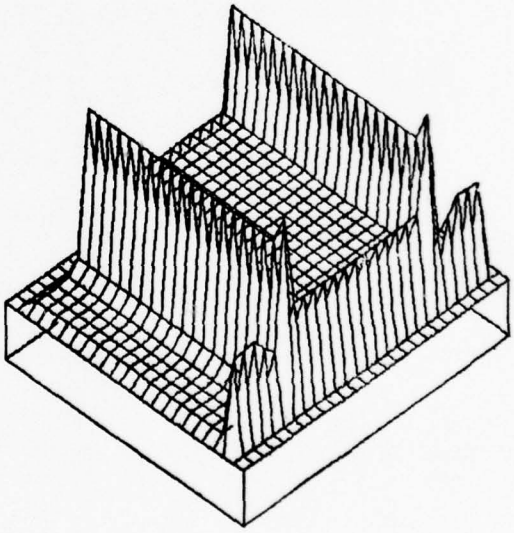


Fig. 12 Temperature profiles of an SOS device through various stages of filamentation. Hot spot formation occurs at time = 7.9 μs. I_{tot} = 25 mA, ND = 1 x 10^{22} m^{-3}, k_e = .08 watt/(m-K).

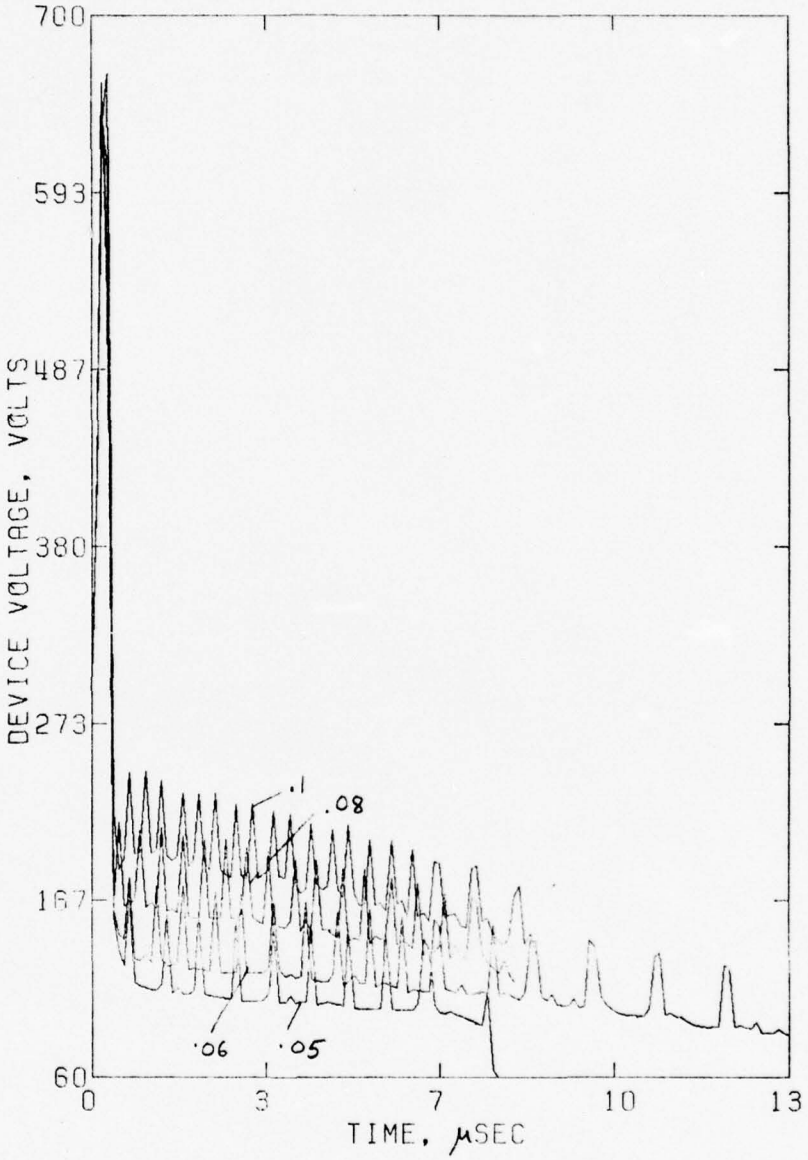
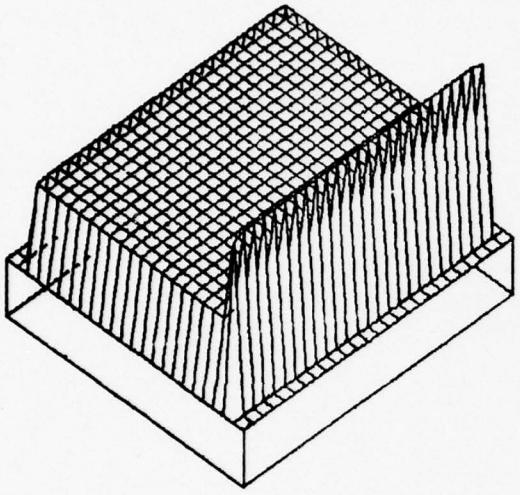
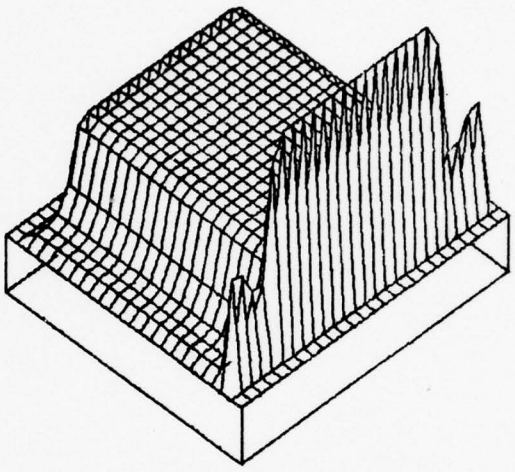


Fig. 13 Terminal voltage as a function of time at a current amplitude of 25 mA for various k_e values. ND = 1 x 10^{22} m^{-3}.

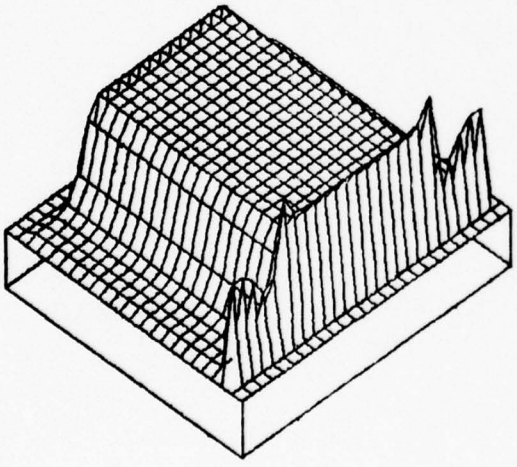
time=.8 μs



time=6.8 μs



time=8.2 μs



time=9.4 μs

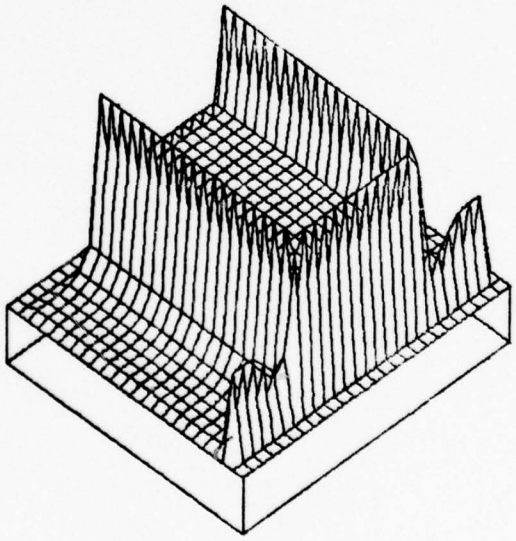


Fig. 14 Changing temperature profiles and double filament formation. I_{tot} = 35 mA, ND = 1 x 10^{22} m^{-3}, k_e = .08 watt/(m-K).

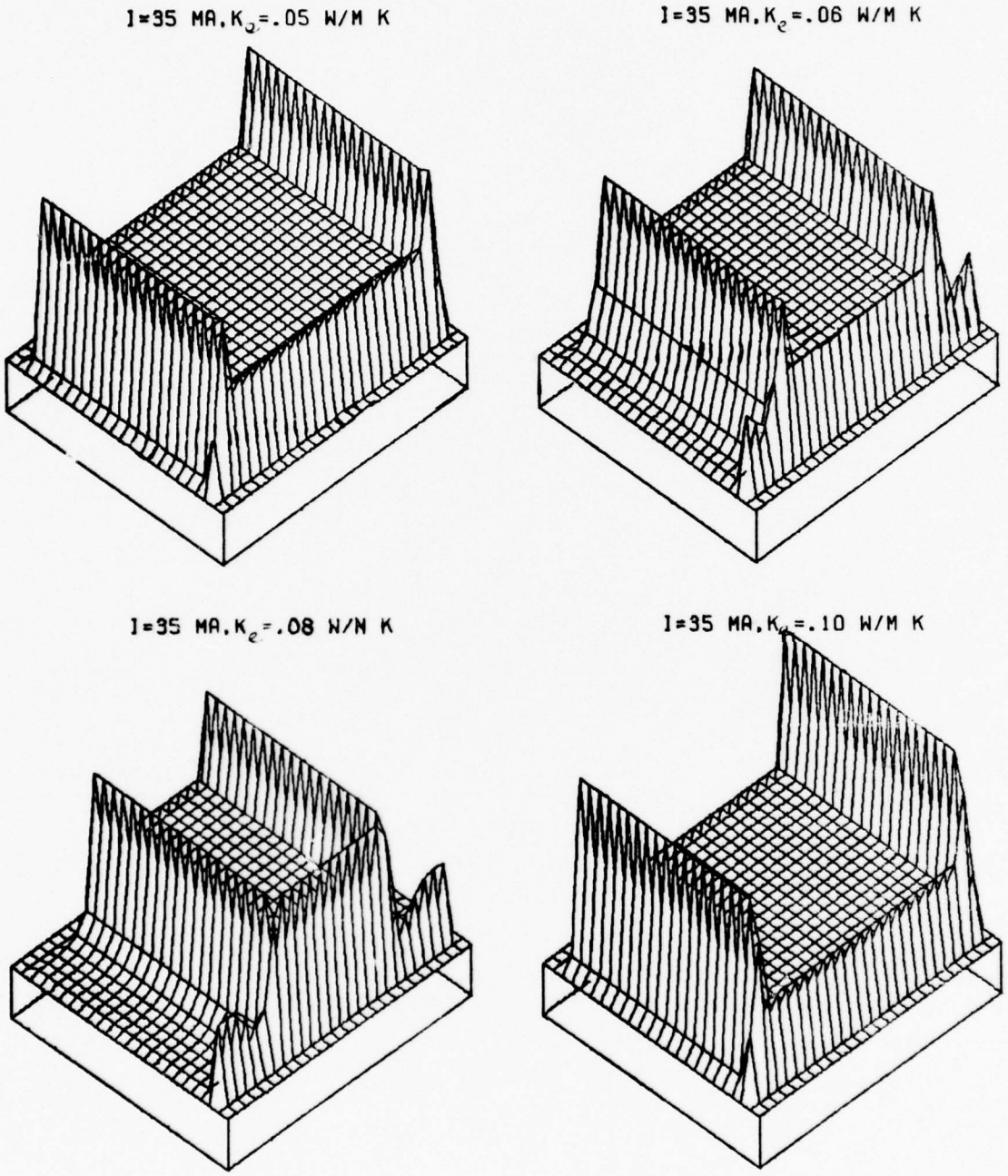
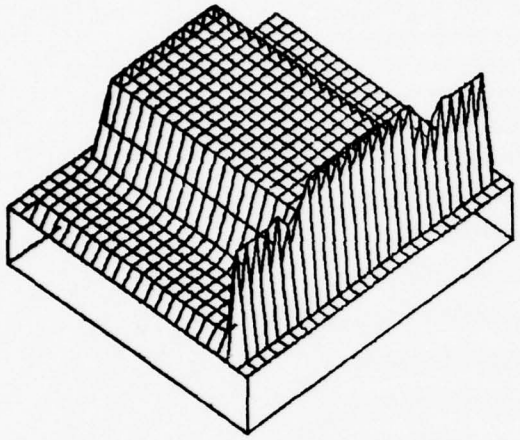
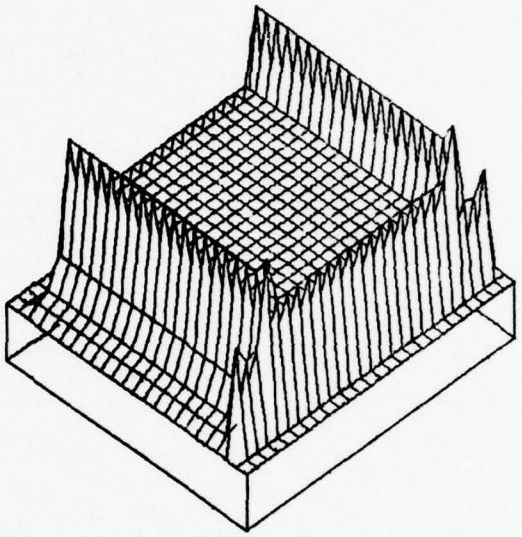


Fig. 15. Dependence of filament multiplicity on k_e. I_{tot} = 35 mA, ND = 1 x 10^{22} m^{-3}

I=15 MA, TIME=14.9E-6S



I=25 MA, TIME=7.5E-6S



I=35 MA, TIME=6.3E-6S

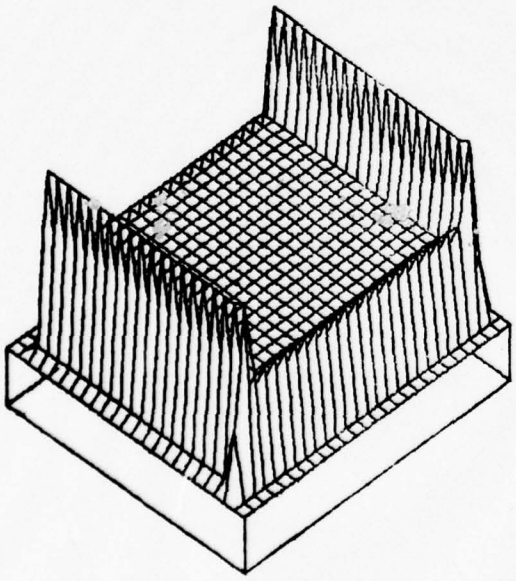


Fig. 16. A comparative study of the influence of pulse amplitudes on the filamentation process. ND = 1×10^{22} m^{-3}

The role of the thermal transfer parameter k_e on filamentation was explored. Representative results are presented here using the diodes with k_e = 0.05, 0.07, 0.08 and 0.10 and current amplitudes of 25 and 35 mA. As shown in Fig. 11, single and double filaments form, depending on the size of k_e. As k_e increases the spacing between the filaments first decreases and then increases, eventually disappearing at the edges of the diode with a single filament appearing at the center of the device. Figure 12 shows temperature profiles at different times for k_e = 0.08 and step amplitude of 25 mA.

Voltage waveforms are shown in Fig. 13 for each of the cases of Fig. 11. The oscillations indicate an error in the program yet to be located. These oscillations raise questions on the reality of the double filaments. Possibly a fluctuation in the solution has caused a momentary hot spot to form in the junction and initiated a filament there when none should exist. Thus a careful examination of the calculation procedure is needed and is underway.

The double filaments persist at different k_e-values for a current pulse amplitude of 35 mA. For k_e = 0.08, the distance between filaments is 44 μm and each is 24 μm from the nearest edge. Figure 14 shows temperature profiles at differnt times for k_e = 0.08 and 35 mA pulse amplitude. When k_e = 0.10, the separation increases to 60 μm and the distance of each from the nearest edge is 20 μm. Figure 15 shows the change in double filament separation with increasing k_e.

Finally, Fig. 16 shows temperature profiles for a single value of k_e and current amplitudes of 15 mA, 25 mA and 35 mA.

Figures 8, 11, 12, 14, 15 and 16 suggest that two important features are missing in the present model, namely the initial localization of the filament at the junction and the convergence of current lines through this junction hot spot. With the convergence is a spreading resistance that is not included in the present model. In the experiments, each filament grew from a junction hot spot and across the n-region, with a well-defined boundary between the hot filament and the cooler surrounding portion of the n-region. The present model, with its multiple segments in the n-region, was proposed having as one of its goals the ability to describe the growth of a filament across the n-region. The model has failed to live up to this expectation up to the present time. However, it is possible that a more careful treatment of the thermal portion of the problem and elimination of the spurious oscillations that appear so vividly in the voltage waveforms of Figs. 9 and 13 may alter things. The results of the model at present are realistic in several ways: it shows the high temperature of the junction region, formation of a filament in a homogeneous (defect-free)

diode, the abrupt transition to a filament accompanied by a junction hot region, a cooler junction region adjacent to a junction hot spot, and a voltage waveform having the appropriate general shape.

At present the model is being pursued in the following ways.

1. To eliminate the spurious oscillations of the voltage waveform.

2. To look more critically at the role of the thermal parameter k_e.

3. To incorporate junction irregularities to simulate diffusion spikes.

4. To investigate filamentation with a external circuit having a constant voltage step and constant impedance.

5. To investigate the effect of double pulses - both step-up and step down.

IV. MILESTONES FOR 1978-1979 PROGRAM

In a research program it is difficult to anticipate the time required to obtain results of appropriate depth. The objectives of the present program are such that each diode test has implications on a number of objectives. Thus the working strategy will be to perform a wide range of tests between June and September of 1978 (when the bulk of our manpower will be available), then to devote the remainder of the time on follow-up experiments and analysis.

The analysis of the experiments can be divided into four sections:

1. Homogeneous diodes--roles of diode width, length of n region, doping, and the inter-relationships of these. External parameters include pulse duration and external circuital constraints.

2. Diodes with specially introduced spikes--roles of spike geometry, n-region length, doping, and the inter-relationships of these. External parameters include pulse duration and external circuital constraints.

3. Current crowding geometries--roles of the type of geometric variation, diode width, n-region length, doping, and the inter-relationships of these. External parameters include pulse duration and external circuital conditions.

4. Development of a screening test for second breakdown susceptibility.

In addition, the theoretical treatment of current filamentation using the model presented in Sec. III, with extensions to include junction spikes, will be further pursued.

APPENDIX A. ONE DIMENSIONAL ANALYSIS OF P-N JUNCTIONS

Voltage-current characteristics and electric field and related profiles of silicon p+ - n abrupt junctions under isothermal, steady state conditions were investigated. Solutions were obtained for current densities between 10^7 and 10^{10} A/m^2, doping densities of the n-region of 10^{20} to 5 x 10^{23} atoms/m^3, and temperatures of 200 to 1600 K. The present work was confined to non-punch-through diodes (i.e., diodes in which the width of the n region is greater than the junction width).

A. Development of pertinent equations

The size of the space charge region of a p-n junction depends on the concentration gradient associated with the uncompensated donors and acceptors and the strength of the applied electric field. The junction region is an electric dipole in an otherwise neutral system. As a result of the high doping density (about 10^{26} atoms/m^3) on the p+ region, this region contains a dense negative space charge within an extremely narrow layer (10^{-10} m) adjoining the junction. On the other hand, the space charge region in the more lightly doped n-region may extend many micrometers from the metallurgical junction. Thus the behavior of an abrupt p+ - n junction is determined by its n-region. At high current densities, mobile carriers can appreciably modify the space charge distribution within the junction.

The junction behavior is determined by the following equations.

Poisson's Equation:

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon} = \frac{q}{\varepsilon}\left(p - n + N_D - N_A\right), \qquad (1)$$

where

- E x-component of the electric field
- x space coordinate
- ρ total charge density (charge/volume)
- ε dielectric permittivety
- q magnitude of the electronic charge
- p charge density of holes
- n charge density of electrons
- N_D charge density of ionized donors
- N_A charge density of ionized acceptors

Continuity equation (including thermal generation and recombination and avalanche generation)

$$\frac{dJn}{dx} = q\,(U - G) \tag{2}$$

$$\frac{dJ_p}{dx} = q\,(G-U) \tag{3}$$

where

J_n electron current density

J_p hole current density

U thermal rate of generation and recombination of electron-hole pairs

G avalanche rate of generation of hole-electron pairs

The functions J_n, J_p, U and G are taken to be

$$J_n = q|V_n|n \tag{4}$$

$$J_p = q|V_p|p \tag{5}$$

$$U = \frac{q\,(n_i^2 - np)}{(p+n_i)\tau_n + (n+n_i)\tau_p} \tag{6}$$

$$G = \alpha_n|V_n|n + \alpha_p|V_p|p \tag{7}$$

where

$|V_n|$ average speed of electrons in a field E

$|V_p|$ average speed of holes in a field E

n_i intrinsic equilibrium carrier density at temperature T

τ_n lifetime of excess electrons in the n region

τ_p lifetime of excess holes in the n region

α_n avalanche coefficient for the generation of electron-hole pairs by an incident electron

α_p avalanche coefficient for the generation of electron-hole pairs by an incident hole

The current densities J_n and J_p combine to give the total current density, J, that is

$$J = J_n + J_p \tag{8}$$

The particle velocities and avalanche coefficients are functions of electric field and of temperature. However, the temperature dependence of the particle velocities has not been included. The functions used for $|V_n|$, $|V_p|$, α_n and α_p are:

$$|V_n| = 1.45 \times 10^2 \, E^{.1525} \quad \text{(MKS)} \quad \text{for } E>10^5 \text{ v/m} \tag{9}$$

$$|V_p| = 4.68 \times 10^4 \, E^{.445} \quad \text{(MKS)} \quad \text{for } E>10^5 \text{ v/m,} \tag{10}$$

from reference 23 and

$$\alpha_n = \frac{1}{\lambda_n} \exp \{(11.5\, r^2 - 1.17\, r + 3.9 \times 10^{-4})\, x_n^2 + (46 r^2 - 11.9\, r + 1.75 \times 10^{-2})\, x_n\} \tag{11}$$

$$\alpha_p = \frac{1}{\lambda_p} \exp \{(11.5\, r^2 - 1.17\, r + 3.9 \times 10^{-4})\, x_p^2 + (46\, r^2 - 11.9\, r + 1.75 \times 10^{-2})\, x_p\}. \tag{12}$$

from reference 24

where

$$\lambda_n = (76 \times 10^{-10} \tanh \frac{Er}{2kT})^{-1}$$

$$\lambda_p = (47 \times 10^{-10} \tanh \frac{Er}{2kT})^{-1}$$

$$r = \frac{\langle Er \rangle}{Ei}$$

$$x_n = \frac{Ei}{qE\lambda_n}$$

$$x_p = \frac{Ei}{qE\lambda_p}$$

$$\langle Er \rangle = Er \tanh \frac{Er}{2kT}$$

$$Ei = 3/2\, Eg$$

Er energy of Raman optical phonon (.063 eV)

The lifetimes, τ_n and τ_p, were taken to be equal and constant.

$$\tau_n = \tau_p = 1 \times 10^{-6} \text{ s} \tag{13}$$

The intrinsic carrier density n_i is

$$n_i^2 = k_i T^3 \exp(-Eg/kT) \quad , \tag{14}$$

where

$k_i = 1.5 \times 10^{45}\ m^{-6}\ K^{-3}$

T temperature

E_g band gap in silicon (1.106 eV)

k Boltzmann's constant

The continuity equations employed, Eqs. 2 and 3, do not contain the time derivatives, $\frac{\partial n}{\partial t}$ and $\frac{\partial p}{\partial t}$, respectively. Thus, steady state solutions are obtained. Diffusion terms have not been included in Eq. 4 and 5.

Eliminating J_p using Eq. 8, Eqs. 1 and 2 become

$$\frac{dE}{dx} = \frac{1}{\varepsilon}\left\{\frac{J}{vp} + \left(\frac{1}{V_n} - \frac{1}{V_p}\right) Jn\right\} + 1.5 \times 10^{-9} (N_D - N_A) \tag{15}$$

$$\frac{dJn}{dx} = \{(\alpha_n - \alpha_p) Jn + \alpha_p\} + U \tag{16}$$

At the boundary, $J_{no} = J - J_{po}$ (17)

These are then solved simultaneously to obtain field and related profiles as a function of distance from the junction, temperature and applied current density.

Figures 17 and 18 show carrier velocities and ionization coefficients, respectively, as a function of electric field. The avalanche coefficients must be greater than 10^6 for avalanche to be an important process. This occurs at fields of $3 - 5 \times 10^7$ V/m.

In reverse bias and moderate temperatures, the current in the junction is provided by carriers created by the avalanche mechanism. The avalanches are initiated primarily by minority carriers that enter the junction from the n-region. For large avalanche currents, the junction characteristics are very insensitive to the size of the entering minority carrier current density J_{po}. However, at elevated temperatures J_{po} increases by orders of magnitude and eventually becomes comparable to the total junction current. Then avalanche becomes less and less important and the junction voltage drops. The temperature dependence of J_{po} is given in Eqs. 18-20 (Ref. 25).

$$J_{po}(T) = qE\mu_p(T)\, p(T) \tag{18}$$

where (using MKS units),

$$\mu_p(T) = \frac{7.55 \times 10^4 \, T^{-5/2}}{\left[1 + \frac{N_D}{\frac{N_D}{81} + 4 \times 10^{16}} + \frac{\frac{E^2}{(6.1\times10^3)^2}}{\frac{E}{6.1\times10^3} + 1.6} + \frac{E^2}{(2.5\times10^4)^2} \right]^{1/2}} \quad (19)$$

and

$$p(T) = -\frac{N_D}{2} + \frac{N_D^2}{2} + n_i^2 \,(T)^{1/2} \quad (20)$$

The junction behavior at different temperatures depends primarily on the temperature dependence of the avalanche coefficients as given in Eqs. 11 and 12 and the temperature of J_{po} as given in Eq. 18-20.

B. Computer simulation procedure

Computer simulations were done on an IBM 370/158 machine using the fourth order Runga-Kutta double precision method of integration and CSMP3 as the main programming language. To solve the relevant differential equations simultaneously, a particular starting value of each of the variables J, T, N_D and J_n were chosen. Integration was started at a point in the n region which was assumed to be the edge of the depletion region. The field at this point is the same as that in the remainder of the n-region. For a current density J, this boundary field is $E_b = \frac{J}{\sigma}$. Here σ is the conductivity of the n region. The minority carrier density at the edge of the junction in the n region is J_{po} and the corresponding boundary value for use in Eqs. 15 and 16 is the J_{no} identified in Eq. 17.

The relationships between carrier velocities and electric field that were used are shown in Fig. 17. This does not include the saturation effect observed experimentally (26, 27, 28). In future work the carrier velocity - electric field curves of Ref. 26-28, shown in Fig. 18, will be used. Spot checks indicate the solutions are not very sensitive to the differences between the curves of Figs. 17 and 18 in fields around 10^7 V/m, the region of greatest concern in the avalanche process.

Figure 19 shows the electric field dependence of the avalanche coefficients. Below 10^6 V/m, avalanche is unimportant. Maximum junction fields are in the 10^7 V/m range.

The electric field in the junction is shown as a function of distance in the n-region from the metallurgical junction in Fig. 20 for $N_D = 10^{21}$, 10^{22}, and 10^{23} atoms/m^3, current density of 10^8 A/m^2, and temperature of 300 K. The size and configuration of the junction field depends upon current density as illustrated in Fig. 21 for $N_D = 10^{22}$ atoms/m^3 and temperature 300 K. The effect of junction temperature on electric field profile is presented in Fig. 22 for $N_D = 10^{22}$ atoms/m^3 and current density 10^8 A/m^2.

Figures 23, 24, and 25 explore the dependence of junction width on n-region doping concentration, current density and temperature, respectively.

J-V-T characteristics are given in Fig. 26 for $N_D = 10^{22}$ atoms/m^3 in the high current density regime that is of concern in reverse- bias second breakdown phenomena.

Finally, Fig. 27 illustrates the dependence of junction voltage on doping density for a current density of 10^8 A/m^2 and a temperature of 300 K.

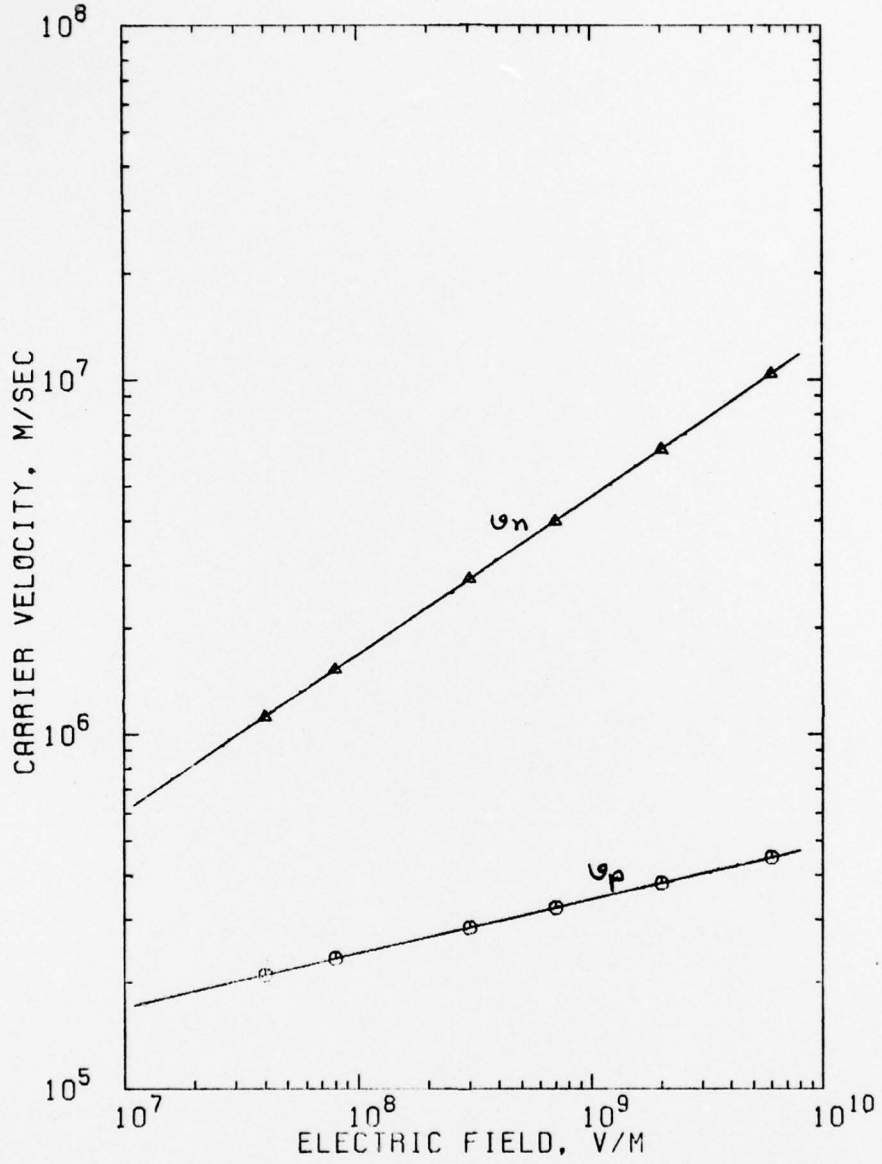


Fig. 17 Electron(v_n) and hole(v_p) drift velocities as a function of the electric field.

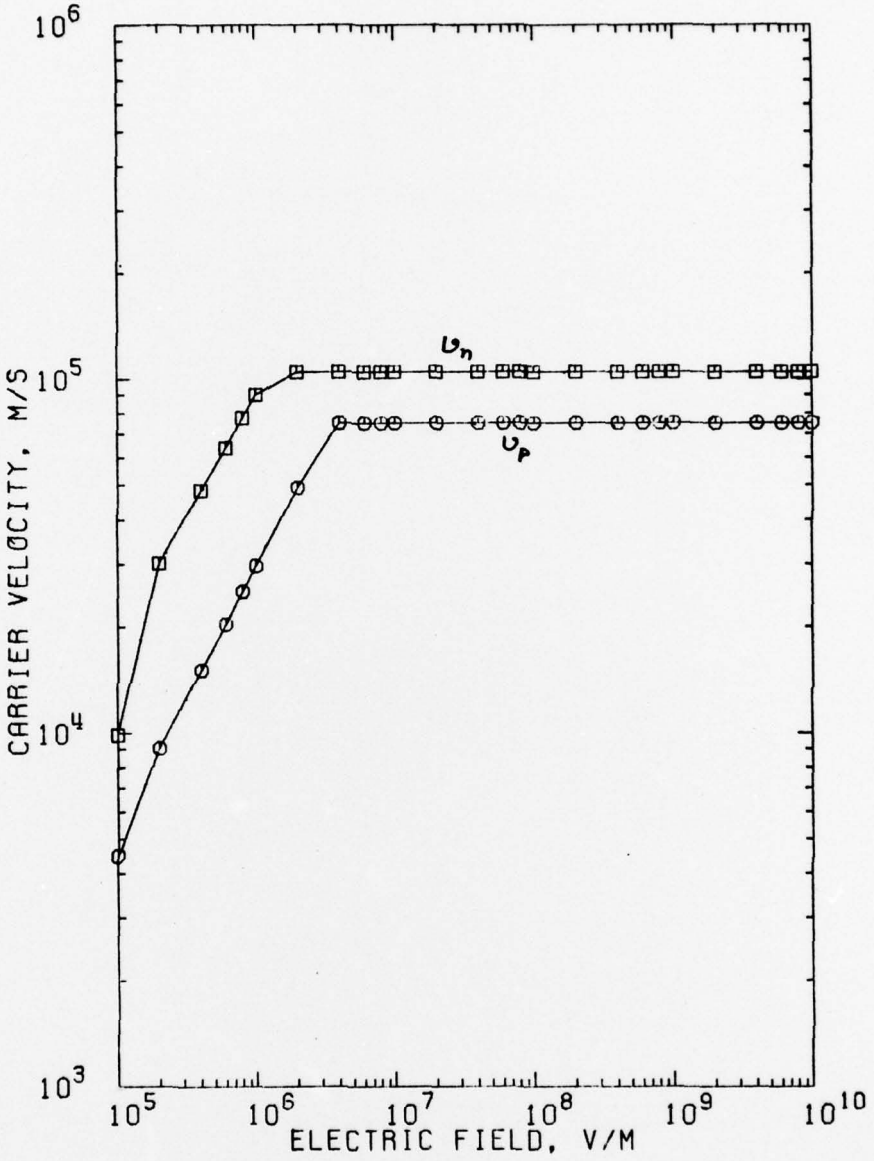


Fig. 18 Electron and hole drift velocities as a function of electric field from Ref. 26-28.

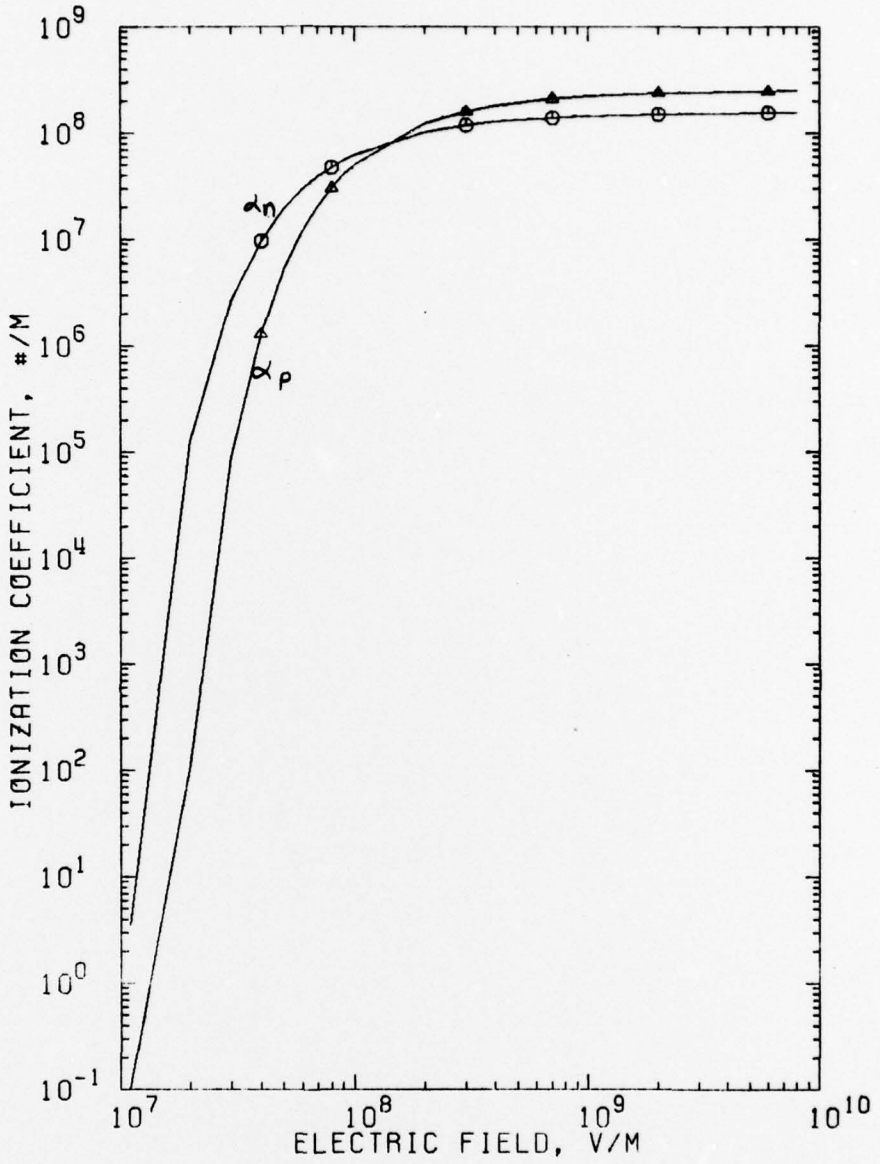


Fig. 19 Electric field dependence of the avalanche ionization coefficients α_n(electron) and α_p(hole) at 300 K.

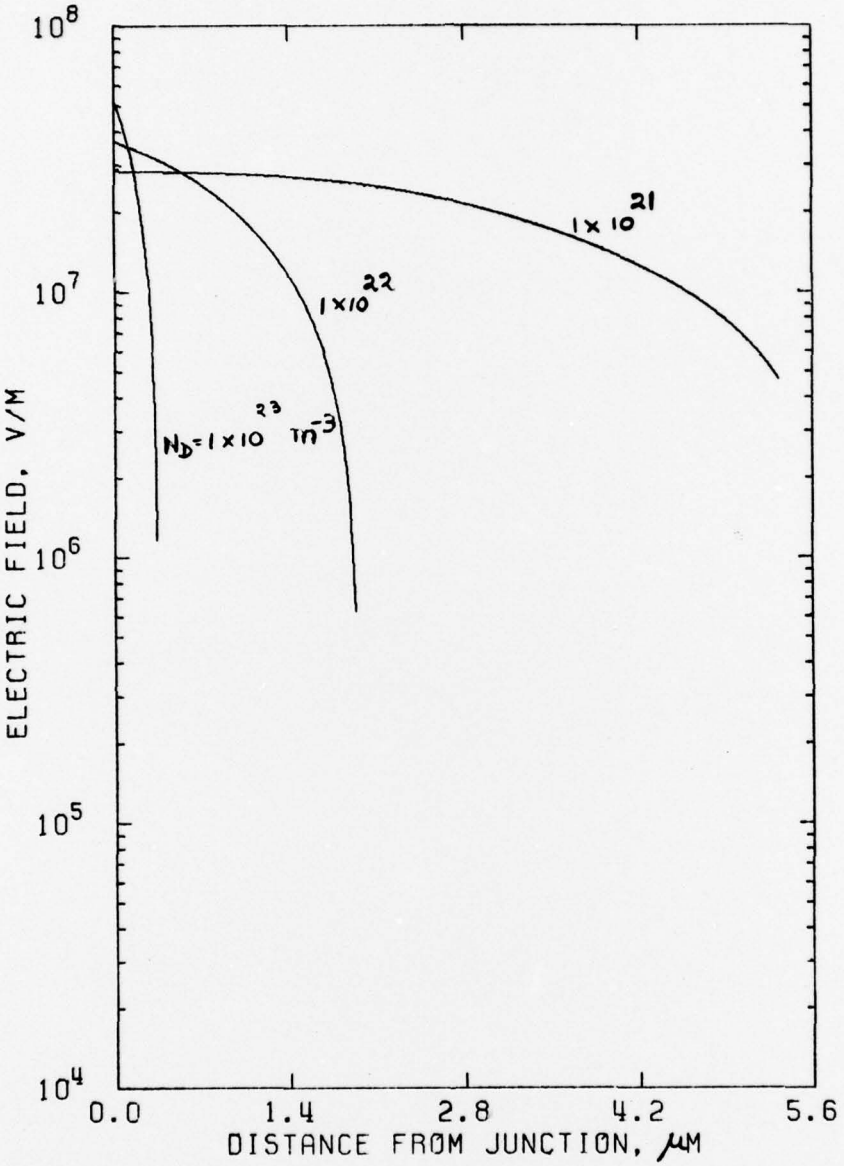


Fig. 20 Electric field as a function of distance from a $p^+ - n$ junction for various doping densities. T = 300 K, $j_{applied} = 1 \times 10^8$ A/m^2.

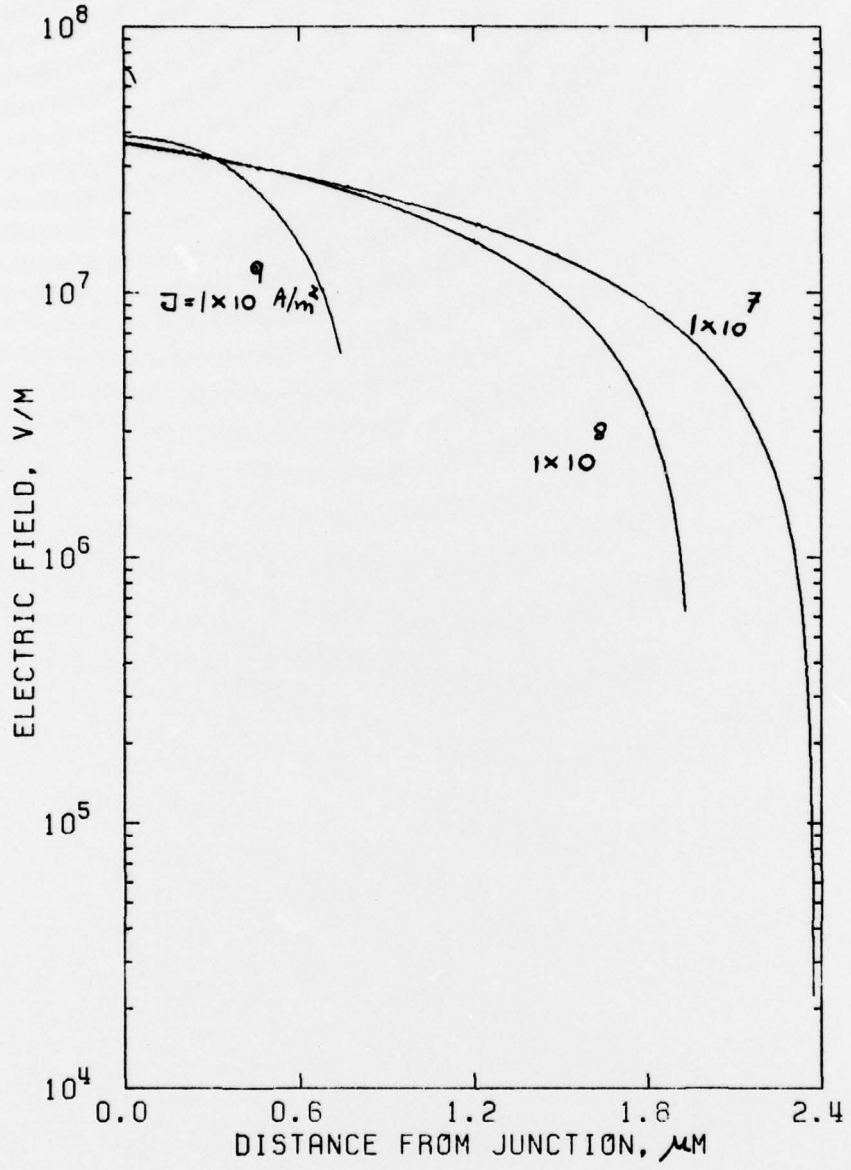


Fig. 21 Electric field as a function of distance from a p+ - n junction at various applied pulse amplitudes($j_{applied}$). T = 300 K, ND = 1 x 10^{22} m^{-3}

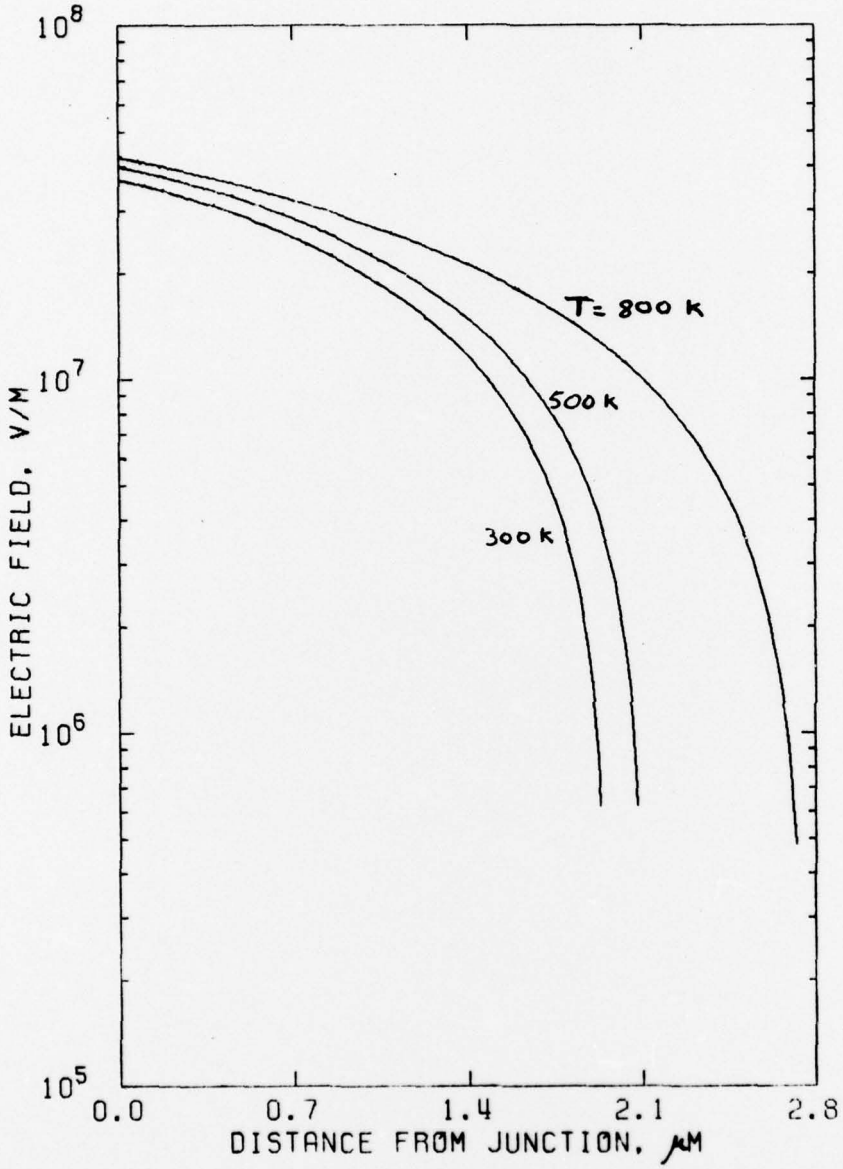


Fig. 22 Electric field as a function of distance from p+ - n junction at various temperatures. ND = 1 x 10^{22} m^{-3}, $j_{applied}$ = 1 x 10^8 A/m^2.

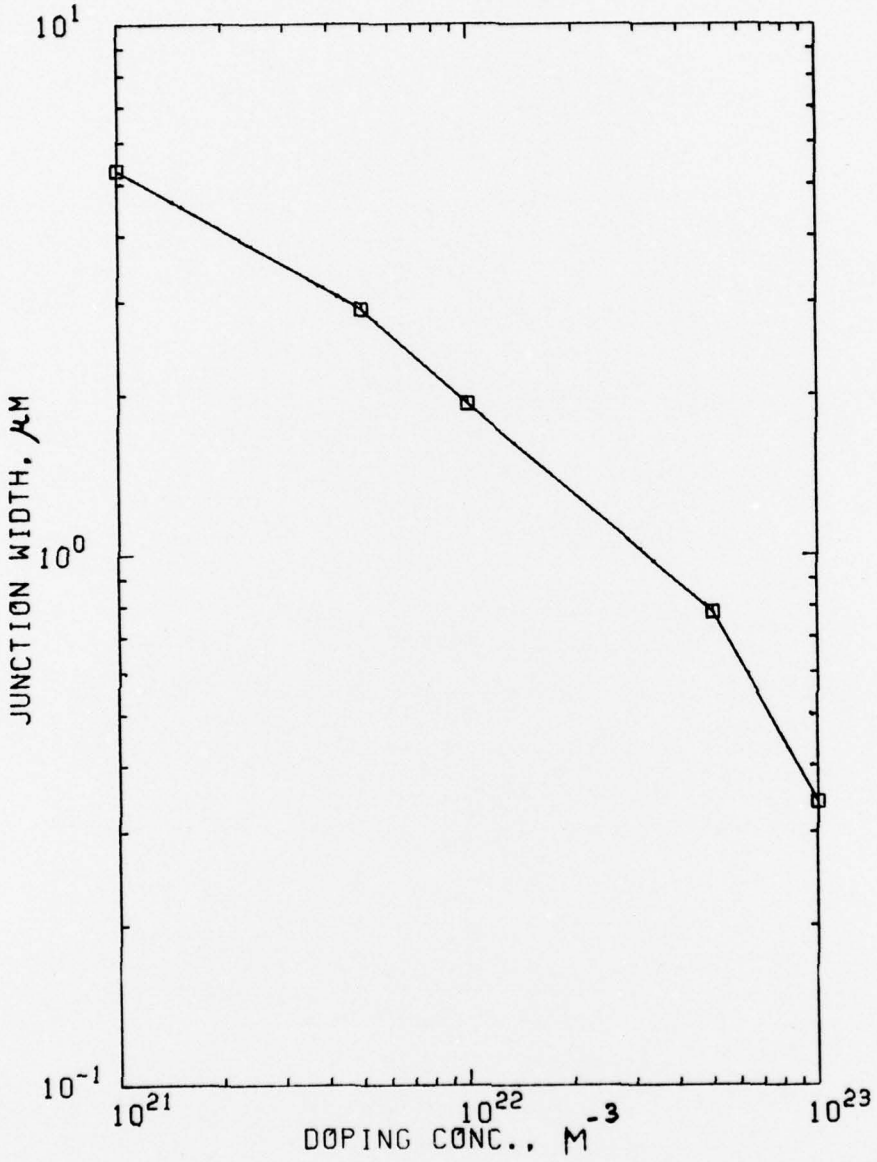


Fig. 23 Junction width as a function of doping density. T = 300 K and $j_{applied} = 1 \times 10^8$ A/m^2 .

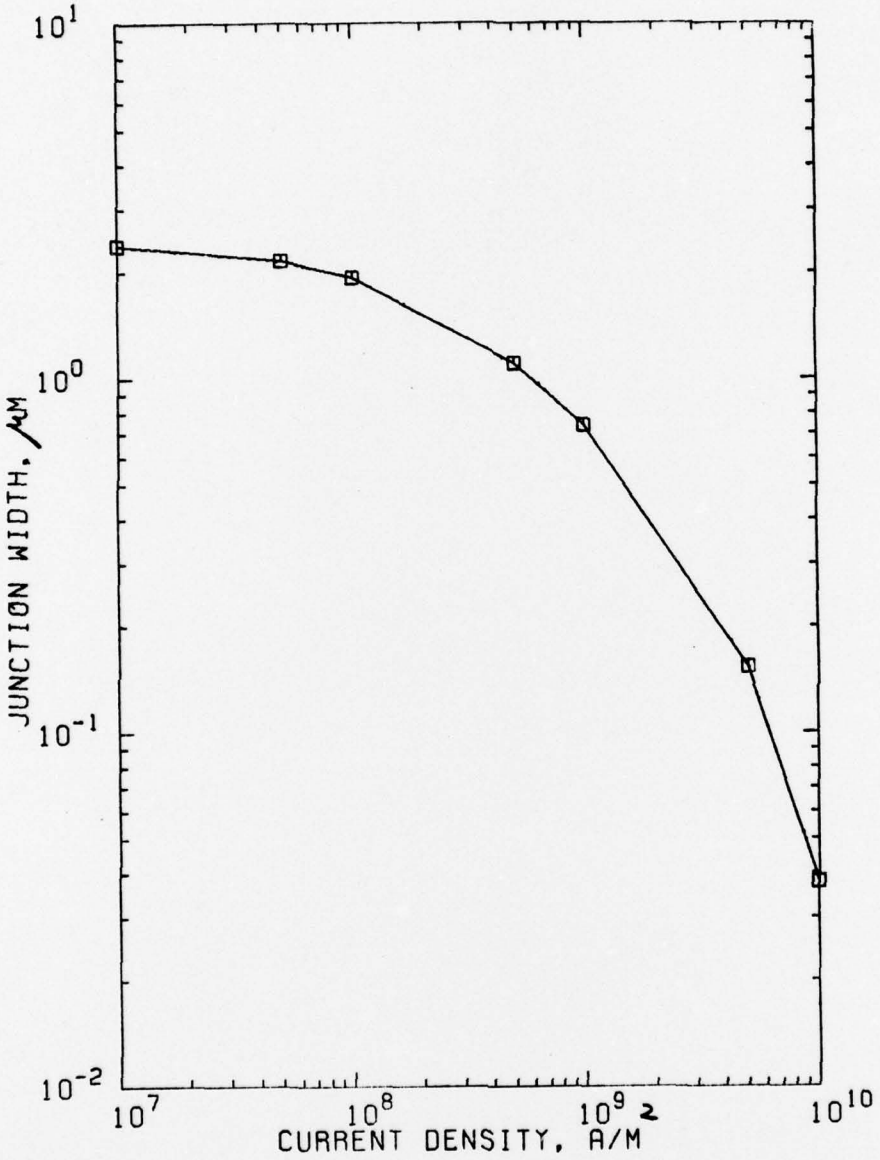


Fig. 24 Junction width as a function of applied pulse amplitudes. T = 300 K, ND = 1 x 10^{22} m^{-3}.

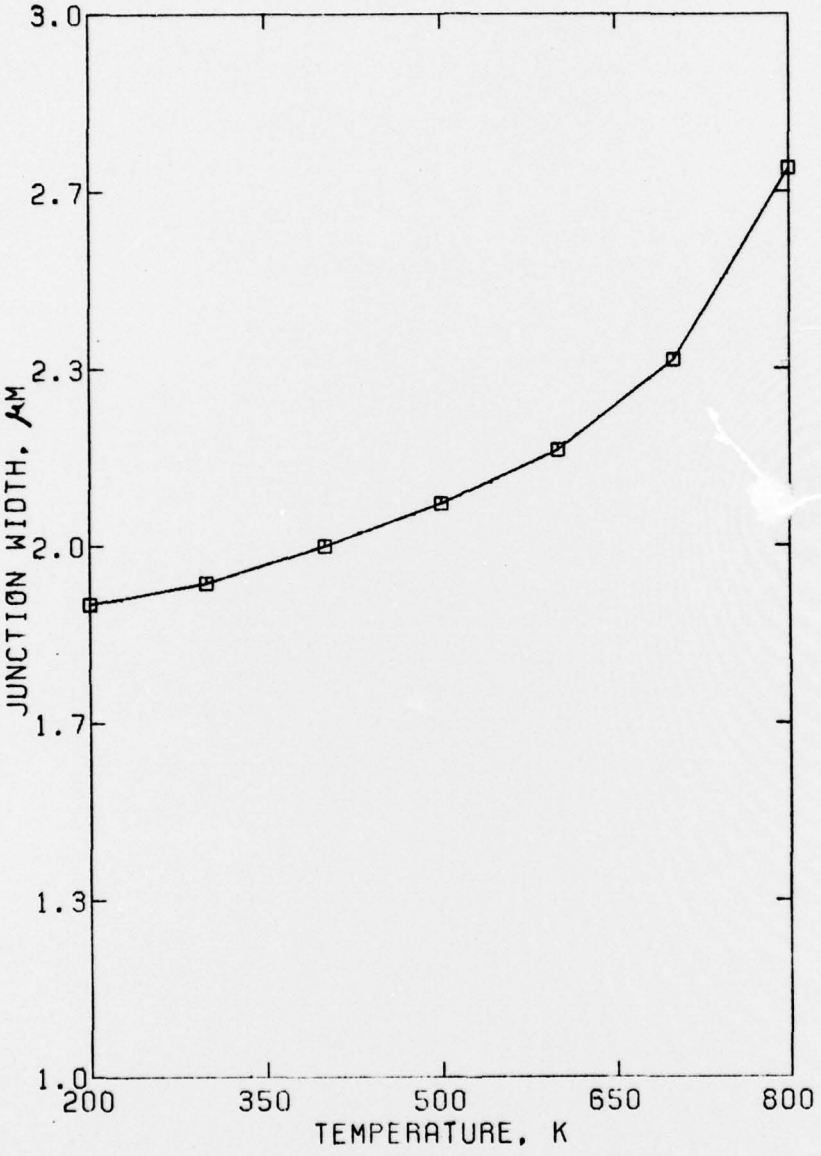


Fig. 25 Junction width as a function of device temperature. $j_{applied}$ = 1×10^{8} a/m^2 and ND = 1×10^{22} m^{-3}.

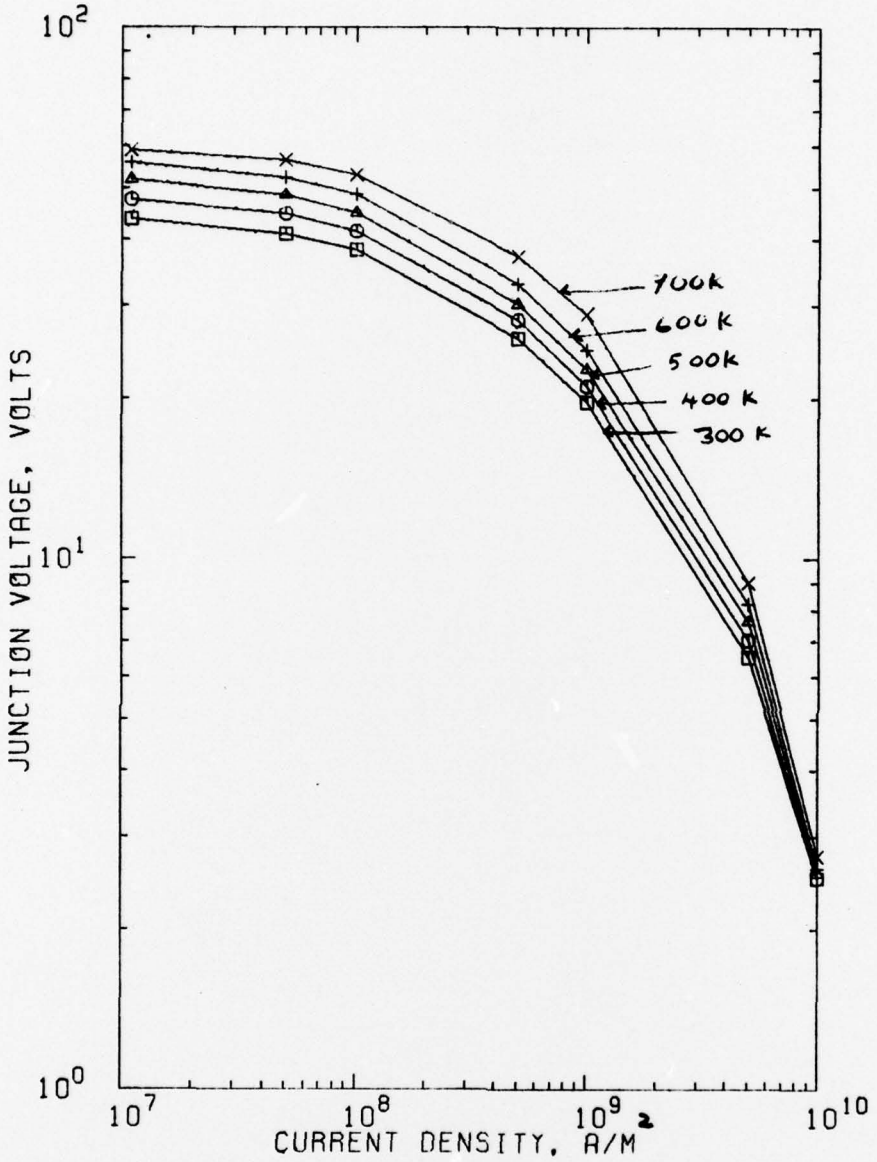


Fig. 26 Junction voltage - current density characteristics at various device temperatures. ND = 1 x 10^{22} m^{-3}.

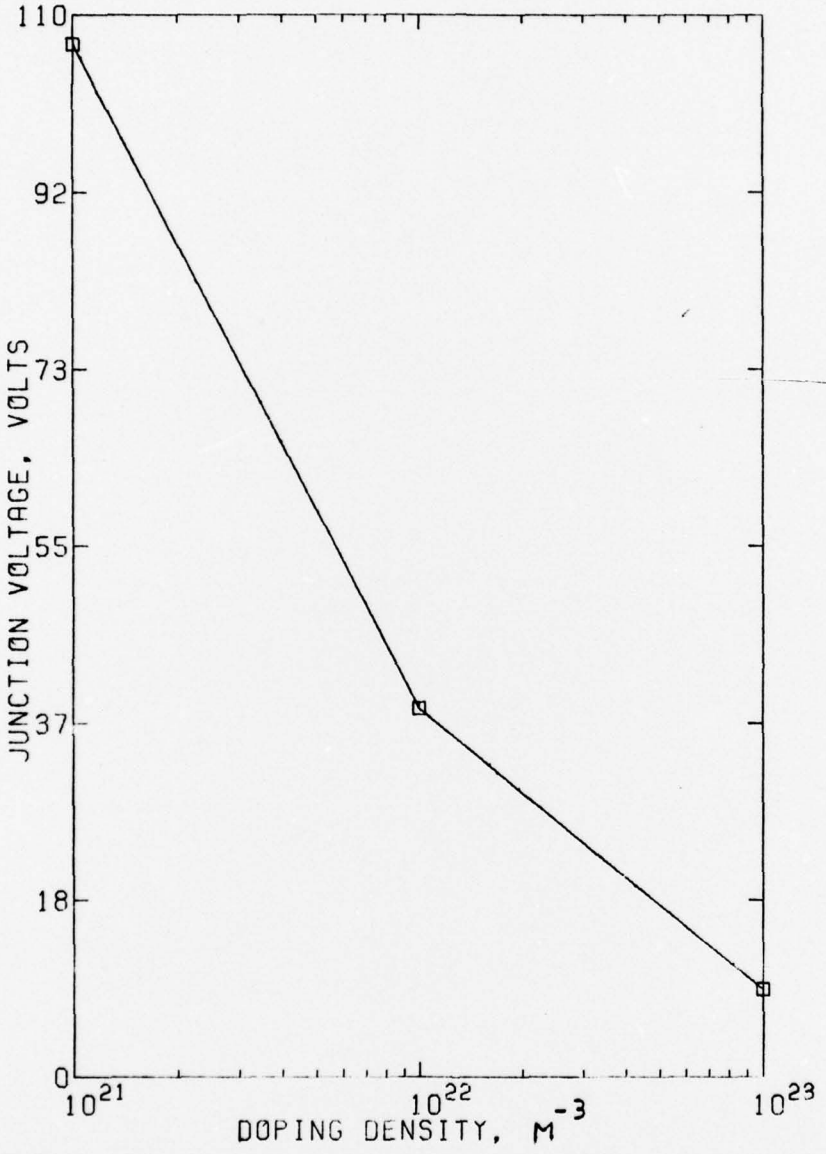


Fig. 27 Junction voltage as a function of doping density. T = 300 K and $j_{applied} = 1 \times 10^{8}$ A/m^{2} .

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